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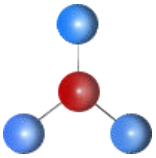

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Welcome to the official website of the International Conference on Electrical and Electronics Engineering (ICEEE). ICEEE aims to bring together researchers, scientists, engineers, and scholar students to exchange and share their experiences, new ideas, and research results about all aspects of Electrical and Electronics engineering and Technology, and discuss the practical challenges encountered and the solutions adopted. The conference will be held every year to make it an ideal platform for people to share views and experiences in Electrical and Electronics Engineering and related areas.

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Editorial

Although the discipline like electrical engineering has narrated academic maturity in the last decades, but the limitations of the non renewable energy sources, turbulence and disturbances in the energy propagation cascades various insightfulness and stimulation in post classical electrical era. Evidence shows that there are phenomenal supplements in power generation and control after the introduction of Energy Management System (EMS) supported by Supervisory Control and Data Acquisition (SCADA). As there is increasing focus on strengthening the capacity of the power houses with the existing resources or constraints some new dimensions like FACTS, Optimal System Generation, High Voltage DC transmission system, Power Generation Control, Soft Computing, Compensation of transmission line, Protection scheme of generator, Loss calculation, economics of generation, fault analysis in power systems are emerging. Since the world is suffering with water, food, and energy crisis, energy consumption has social relevancy.

Keeping view of the ongoing energy and power issues many action research can be initiated by the research fraternity of this domain. The conference is a thought provoking outcome of all these interrelated facts.

In the quest of making this earth a better place to live we have to make a strong hold upon sustainable energy source. Sustainable energy sources include all renewable energy sources, such as hydroelectricity, solar energy, wind energy, wave power, geothermal energy, bioenergy, and tidal power. It usually also includes technologies designed to improve energy efficiency. Energy efficiency and renewable energy are said to be the twin pillars of sustainable energy. Renewable energy technologies are essential contributors to sustainable energy as they generally contribute to world energy security, reducing dependence on fossil fuel resources, and providing opportunities for mitigating greenhouse gases.

Let me highlight some of the recent developments in Electronics discipline. The new integrated devices did not find a ready market. Users were concerned because the individual transistors, resistors, and other electronic circuit components could not be tested individually to ensure their reliability. Also, early integrated circuits were expensive, and they impinged on the turf that traditionally belonged to the circuit designers at the customer's company. Again, Bob Noyce made a seminal contribution. He offered to sell the complete circuits for less than the customer

could purchase individual components to build them. (It was also significantly less than it was costing us to build them!) This step opened the market and helped develop the manufacturing volumes necessary to reduce manufacturing costs to competitive levels. To this day the cost reductions resulting from economies of scale and newer high-density technology are passed on to the user—often before they are actually realized by the circuit manufacturer. As a result, we all know that the high-performance electronic gadget of today will be replaced with one of higher performance and lower cost tomorrow.

The integrated circuit completely changed the economics of electronics. Initially we looked forward to the time when an individual transistor might sell for a dollar. Today that dollar can buy tens of millions of transistors as part of a complex circuit. This cost reduction has made the technology ubiquitous—nearly any application that processes information today can be done most economically electronically. No other technology that I can identify has undergone such a dramatic decrease in cost, let alone the improved performance that comes from making things smaller and smaller. The technology has advanced so fast that I am amazed we can design and manufacture the products in common use today. It is a classic case of lifting ourselves up by our bootstraps—only with today's increasingly powerful computers can we design tomorrow's chips.

It’s my pleasure to welcome all the participants, delegates and organizer to this international conference on behalf of IOAJ family members. I sincerely thank all the authors for their invaluable contribution to this conference. I am indebted towards the reviewers and Board of Editors for their generous gifts of time, energy and effort.

Editor-in-Chief

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MMSE Based Channel Estimation for Millimeter Wave MIMO System using TSV Model

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Abstract - Millimetre wave communication provides high data rates for communication. MIMO technology is nowadays gaining importance for its capability to meet high data rates. In this paper MIMO channel estimation is done for the indoor environment. The indoor channel is modelled using Triple Saleh Valenzuela(TSV) model, as TSV takes in to account both the Time of arrival of the rays and Angle ofArrival information of the antenna.Channel state informationCSI) is required for transmitter and/or at the receiver for effective performance. Training based channel estimation is done using the MMSE technique. With the knowledge of channel correlation matrix and receiver noise power MMSE provides better performance giving a BER of 10^{-5} at SNR of 7db.

Keywords - *TSV, MIMO, MMSE*

I. INTRODUCTION

Due to the rapid increase in demand for high data rates in wireless communication systems, array-based transceivers and space diversity methods have recently become an widely interested area of research. It has been shown that in rich scattering environments, multiple-input multiple-output (MIMO) techniques can increase the capacity of wireless systems to a great extent. Millimetre wave (MMW) communication provides a great opportunity for high data rate communication. The reason behind this is that the 7GHz in the 57-64 GHz band is allocated for unlicensed use. The opportunities in this particular region of the spectrum include the next generation Wireless personal area network. The millimetre wave systems support a minimum data rate of 1Gbps. However, to make use of advantages that MIMO offers, accurate channel state information (CSI) is required at the transmitter and/or receiver. For instance, the performance of beamforming is entirely determined by the accuracy of the CSI at the transmitter. If space-time coding is used, then accurate CSI at the receiver is important for the decoders. Therefore, accurate channel estimation is very important and plays a key role in MIMO communications.

One of the most widely and popularly used approaches to the MIMO channel estimation is to employ training symbols and then to estimate the channel based on the data received and the knowledge of training symbols.

II. BACKGROUND

Milli-meter waves can be classified as Electromagnetic Spectrum that corresponds to wavelengths from 10mm to 1 mm that sans from 30GHz to 300GHz.. Modelling environment for indoor propagation is complex due to large variation in layout and materials used for construction. Environment can change radically by movement of people, blockage by walls etc. Another important factor to be taken into account for indoor wireless operation is interference. Indoor path loss can change dramatically with either time or position, because of multipath present. The main component of complexity in an indoor propagation arises due to the multipath. This increases the indoor path loss. The wideband of waves used in indoor environment increases the sensitivity to delay spread. Site-specific and Site-general modelling are the two general types of propagation modelling present. Site-Specific modelling requires information from an architectural point of view i.e. information on floors, material used for construction etc. This modelling is generally performed using ray tracing methods. Site-general models give statistical predictions of the path loss for a link design. This model tends to be the more widely used model. Milli-meter Waves are mostly affected by small-scale fading that encompasses the fading that occurs with very small changes in the relative position of the transmitter and receiver and reflectors in the chosen environment.

The channel model that is employed in this paper for the Milli-meter wave propagation in the indoor environment is the Triple Saleh Valenzuela (TSV) model which is a Site general model. This model is contributed by NICT Japan to the 802.15.3c Channel model subgroup. This model is a merger of the two-path model and Saleh-Valenzuela (S-V) model. The Impulse Response of the S-V model takes in to account only the complex amplitude of each ray and the Time of-arrival information of each ray in a cluster. In order to include the effect of antenna, the angle-of-arrival information was also used in the computation of the Complex Impulse Response (CIR), thus the directivity of antenna is convoluted to the S-V component that makes this model a modified form of S-V model. The Power Delay Profiles obtained from the simulations from the model describe different parameters like cluster arrival rate, ray arrival rate, cluster decay rate and ray decay rate and gives a clear picture of the LOS component and the NLOS components present in the environment.

III. TSV CHANNEL MODEL

The proposed model is for indoor environment. So the channel model has to take into account the influence of antenna directivity and the angle of arrival information as well. Saleh- Valenzuela(S-V) channel model does not take into account of those and the influence of antenna is added to the impulse response of S-V model and Triple Saleh Valenzuela (TSV) channel model is considered for the indoor environment.TSV is a combination of Saleh-Valenzuela (S-V) model and the two-path model.

The complex impulse response (CIR) of the TSV channel model is[3]

$$h(t) = \beta\delta(t) + \sum_{l=0}^{\infty}\sum_{m=0}^{\infty}\alpha_{l,m}\delta(t - T_l - \tau_{l,m})\delta(\phi - \psi_l - \psi_{l,m}) \quad (1)$$

Where,

B : direct path component taken into consideration for LOS conditions,

$\alpha_{l,m}$: Complex amplitude of each ray, t is the time of consideration,

T_i: delay time of l^{th}cluster,

ψ_l : Angle of arrival of the l^{th}cluster,

$\psi_{l,m}$: Angle of arrival of the m^{th}ray relative to the first ray in the l^{th} cluster.

Here h(t) is a complex envelope expression of impulse response of the received signal. First part of the equation is direct path component taken from two path model and second part is S-V component.

The direct path β is given by[3]

$$\beta = \frac{\mu_D}{D}\left| G_{t1}G_{r1} + G_{t2}G_{r2}\Gamma_o\left[j\frac{2\Pi}{\lambda_f}\frac{2h_1h_2}{D}\right]\right| \quad (2)$$

Where,

G_{t1}, Gr1are the amplitude of the direction of the direct pass.

$G_{t2,}$ Gr_2 are the amplitude of the direction of the reflection pass (two path model).

$h_{1,}$ h_2 are transmitting and receiving antenna heights.

D is distance between two antennas

μ_d is average value of distribution.

λ_f is wavelength at centre frequency.

In this model, distribution of angle is assumed as Laplacian distribution of equation[3]

$$p(\psi_{l,m}) = \frac{1}{\sqrt{2\sigma}}e^{\frac{\sqrt{2}\psi_{l,m}}{\sigma}} \quad (3)$$

Where σ is the angle spread of rays in the cluster.

The arrival rate of clusters and rays are defined by the poisson process as follows [3]

$$p(T_l \mid T_{l-1}) = \Lambda\exp\{-\Lambda(T_l - T_{l-1})\}\ l > 0 \quad (4)$$

$$p(\tau_l \mid \tau_{l,(m-1)}) = \lambda\exp\{-\lambda(\tau_l - \tau_{l,(m-1)})\}\ m > 0 \quad (5)$$

Where Λ and λ are the cluster and ray arrival rate respectively.

The power delay profile of TSV is shown in figure below.

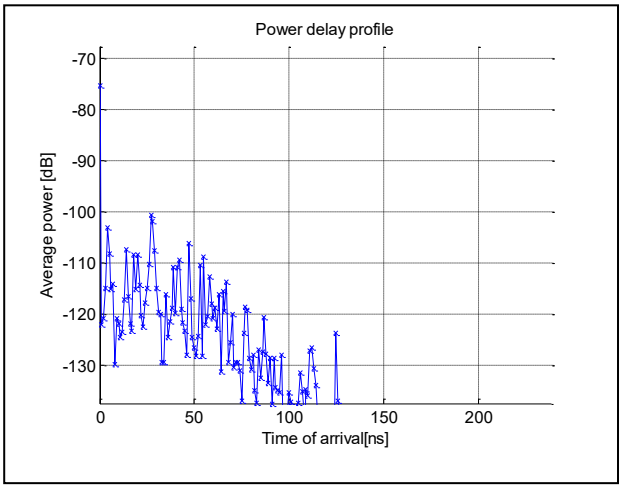

Fig. 1: power delay profile of TSV model

The above figure is the Power delay profile of the TSV model. The one with an average power of around -75db is the LOS component and others constitute the NLOS components. The other details that we obtain are

- Avg RMS Delay 2.69 ns
- Max RMS Delay 10.37 ns
- Max Rician Factor 51.806 db

IV. CHANNEL ESTIMATION

Of the three types of channel estimation methods; blind, semi-blind and training (pilot) method, training or pilot based channel estimation method is usedin this paper. In this method we introduce training bits before actual data in each block and the optimum training required are found out.. . Optimum number of training bits per block is chosen to be equal to number of transmitting antennas [2].Optimum number of training bits is chosen because too much training results in less space for actual to be send and less training results in improper estimation of channeldirectional antenna results in delay spread of few nanoseconds. Such small delay spread results in flat-fading conditions. The channel is assumed to be stationary for a block of data. Using these training bits and output of channel, the receiver estimates the channel. The estimation method for blind and semi-blind are more complicated when compared to training method.. In this paper MMSE technique is used for estimating the channel for the 2x2 system.

Let us consider a MIMO system with M transmitting antennas and N receiving antennas. The Nx1 received signal vector can be expressed as[1]

$$y_i = Hx_i + v_i \qquad (6)$$

Where, x is Mx1transmitted signal vector, H is NxM complex random channel matrix, v is Nx1 noise vector.

The main aim of channel estimation is to find H from the knowledge of Y and X

Linear MMSE estimator H is given by[1]

$$\hat{H}_{MMSE} = Y(X^H R_H X + \sigma^2{}_n rI)^{-1^H} X^H R_H. \qquad (7)$$

Where,

Y is received signal vector, X is training signal vector, $R_H$is channel correlation matrix, I is identity matrix, σ^2 is signal to noise ratio.

V. RESULTS AND CONCLUSION

A 2x2 MIMO system is considered and channel estimation is done using MMSE technique for Indoor environment. The following table shows the simulation parameters used for the proposed model

Table-1

PARAMETER	VALUE
Data rate	10000bps
Channel model	TSV
Transmitter and receiver antenna bandwidth	30^0
Number of channel realizations	2
Distance between transmitter and receiver	3 metres
SNR	-3 to 8 dB

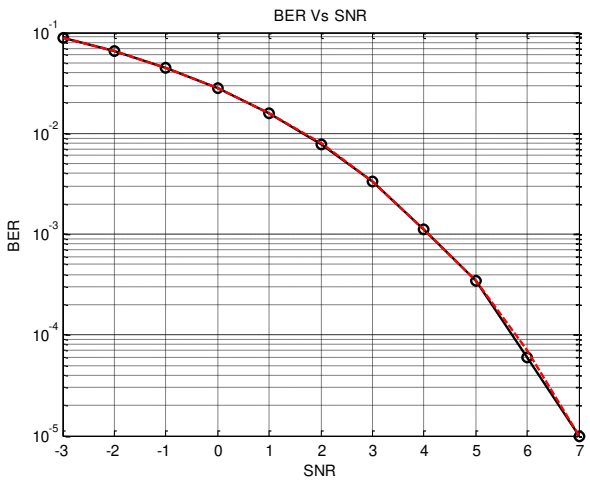

Fig. 2 : BER Vs SNR plot for (2x2) system using MMSE

Channel estimation is done for the Indoor environment using TSV model and performance analysis is done using MMSE estimator. From figure 2,, it is found that at 6 dB, BER is 10^{-4} and at 7 dB, BER is 10^{-5}, as in MMSE.

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Modern Transducers for Measuring High Current in Power System

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Abstract - The accurate and reliable measurement of the system parameters is very essential for safe and stable operation of an electric power system. In particular, current and voltage. Conventionally this has been achieved on high voltage systems by expensive and bulky iron-core transformers. Research effort into viable alternatives to instrument transformers has been ongoing for many years to reduce the cost and improve the safety and accuracy of these devices. This paper proposes an alternative for the measurement of high current by using the piezoelectric technology; Simulations are carried out for the same based on developed algorithm using MATLAB/SIMULINK the successful results in this field have opened the way to propose alternatives for measuring current.

Keywords - *Lead Zirconate Titanate(PZT-5) disc; high current; piezoelectric effect;Measurement; current sensor.*

I. INTRODUCTION

An accurate electric current transducer is one of the key components in power system instrumentation. It provides the current signal source for the revenue metering, control and relaying apparatus. In the measuring, counting, control and protection (relaying) field of power supply, it is well known the need of monitoring the electrical potential and current in the conductors of the transmission lines and the conductors connected to substation power transformers. These measurements are transmitted to a central power station [1,2] for the control of the entire power system to assist the dispatch operator and other bulk network functions depending on the power control centre.

The new requirements of the modern metering and protection systems are based on electronic and microprocessor devices. This trend in the modern systems has forced to the development of novel transducers, where the accuracy, the reliability and safety has been significantly improved. The present paper proposes the new technique in the field of piezoelectric transducers for measuring current [1]. Section II deals with an overview to current transformers. Operating principle of the piezoelectric sensor is presented in section III. In section IV magnetic force appeared in the gap of electromagnet is illustrated. Prototype construction of an electromagnet piezoelectric current sensor and its feature and limitations are discussed in section V and VI respectively. An overview of Two wires piezoelectric transducer is presented in section VII. In section VIII prototype of a Two wires piezoelectric current sensor is discussed. In section IX software design with flowchart of developed algorithm in MATLAB simulation analysis is made and finally conclusion is discussed in section X.

II. CURRENT TRANSFORMERS

Conventional current transducers are transformers (CTs) with copper wire windings and iron cores, and are now widely used in power systems. The reliability of conventional high-voltage CTs has been questioned by engineers at some utility companies who have experienced violent destructive failures of these CTs which caused fires and impact damage to adjacent apparatus in the switch yard, electric damage to relays, and power service disruptions [3-4].

With the short circuit capacities of power systems getting larger and the voltage levels going higher, the conventional CT becomes more and more bulky and costly. Although the introduction of SF6 insulated CTs in recent years has improved reliability, it has not reduced the cost of this type of CT.

With computer control techniques and digital protection devices being introduced into power systems, conventional CTs have caused further difficulties, as they are likely to introduce electromagnetic interference through the ground loop into the digital systems.

Furthermore, the standard 5A low burden secondary configuration is not compatible with the new technology which uses analogue to digital converters requiring low voltage input at the front end. Table 1 shows the reduction on the burden requirements of CTs.

The lower power consumption of the current protection systems and electronic revenue-metering is encouraging and motivating the appearance of new high current transformers. At the same time there are higher demands for operation reliability as a result of interconnection of networks, and an increase in the measuring points is being proposed in the new standards of high voltage networks. Thus, low output (0.5VA) and low cost voltage and current sensors will be necessary.

TABLE I. Current transformer requirements

		Protection Relay	Intermediate Transformer Input	Transfer-system input (losses) (Cable 2×2.3 mm diameter 50 m long)	Current sensor output
		(S3)		(S2)	(S1)
Type of Relay / Static Technology	(1) Electromechanical Relay Technology	1A 10 ... 30 VA 5A 10 ... 30 VA	1 ... 5 VA 1 ... 5 VA	1A :0.5 VA 5A :12 VA	12 ... 36 VA 23 ... 47 VA
	(2) Electronic Analog Relay Technology	1A 1 ... 3 VA 5A 1 ... 3 VA	1 ... 5 VA 1 ... 5 VA	1A :0.5 VA 5A :12 VA	3 ... 9 VA 13 ... 14 VA
	(3) Electronic Digital Relay Technology	1A 0.1 ... 0.5 VA 5A 0.1 ... 0.5 VA	0.1 ... 0.5 VA 0.1 ... 0.5 VA	1A :0.5 VA 5A :12 VA	1 ... 2 VA 13 ... 14 VA
	(4) Microprocessor based Technology	1A 0.1 ... 0.5 VA 5A 0.1 ... 0.5 VA	not necessary	1A :0.5 VA 5A :12 VA	1 VA 13 VA

(Arrows indicate the energy flux from High voltage to low voltage (s1) to (s3))

III. THE PIEZOELECTRIC SENSOR

A. *Principle of operation*

The piezoelectric sensors are based on the principle of electromechanical energy conversion. The mechanical input is converted into electrical output is the basis of these transducers i.e. these transducers exhibit piezoelectric effect Illustrated in Figure1 . [8]

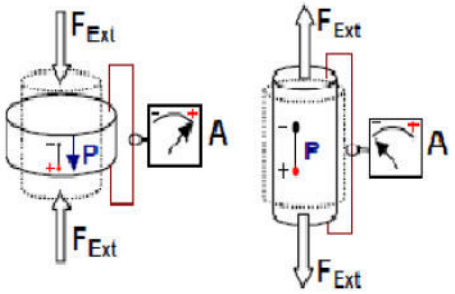

Fig. 1 : Direct effect with piezoelectric material shorted

B. *Piezoelectric effect*

When certain solid materials are deformed, they generate within them an electric charge. The reverse is also true and thus if a charge is applied, the material will mechanically deform in response. These are known as piezoelectric effect [8].

1. *Longitudinal Effects*

If a force is applied to a piezoelectric material along the x-axis, charge is developed on the two faces A and B. The above is known as longitudinal effect.

2. *Transverse effect*

If an electric field acts on a piezoelectric body along the yaxis, charge is developed on the two faces A and B. the above is known as transverse effect.

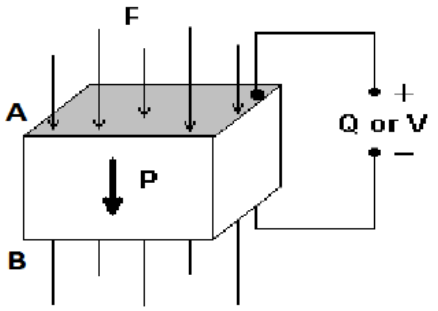

Fig. 2 : Longitudinal effect with the piezoelectric

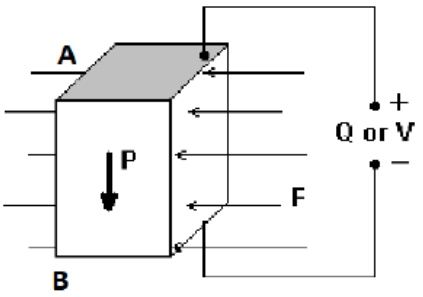

Fig. 3: Transverse effect with the piezoelectric

IV. ELECTROMAGNETIC-PIEZOELECTRIC TRANSDUCER

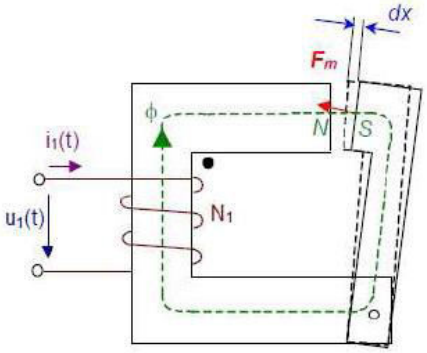

Fig. 4 : Magnetic force appeared in the gap of an electromagnet

An electromagnetic-piezoelectric transducer measures the magnetic force created by means of the magnetic field existing in the gap of an electromagnet and which tends to close it. The magnetic field appears when an electrical current is driven in awinding placed through the core of electromagnet, as is illustrated in Figure 4 [1].

V. CONSTRUCTION OF AN ELECTRO MAGNETIC PIEZOELECTRIC CURRENT SENSOR

A. *Prototype construction*

Figure 5 illustrates a schematic of the prototype developed for testing the electromagnetic piezoelectric current sensor [1].

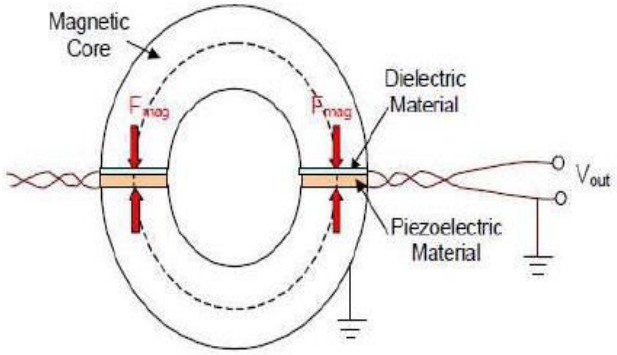

Fig. 5 : Prototype of electromagnetic-piezoelectric current Sensor

This prototype consists of a magnetic core where a wire is wound. The current to be measured is driven through the winding. A piezoelectric sensor is placed in the gap of the electromagnet and all the system is prestressed to allow a good mechanical matching.

When the current to be measured is applied to the winding, the generated force tends to close both the parts of the core of the electromagnet, and thus a compression force appears in the gap. Since the force is quadratic with respect to the current, a compression force will always appear in the gap. The frequency of the measured force is twice the frequency of the primary current and so, the generated voltage will be quadratic with respect to the current.

VI. FEATURES AND LIMITATIONS

In spite of this system presents an interesting alternative for current measurement, their application is limited due to similar problems as the conventional current instrument transformer. This is due to the existence of the magnetic corewhich can be saturated when faults appear.

Nevertheless the existence of the gap increases importantly the limit of the saturation and then the working limit of the transformer compared to the classical transformer, where there is no gap.

Regarding the power required from the source, this might significantly be reduced because power is not necessary for driving the secondary. The output signal in the secondary may drive directly digital electronic circuit as a result of its low power.

The cost and weight of the system is importantly reduced due the non existence of secondary winding. Nevertheless theweight of the core and their dimensions are similar to the electromagnetic current transformer. A most reliable alternative which reduces totally the use of magnetic material (and thus which overcomes the problems of hysteresis, weight and dimensions) is presented below.

VII. TWO-WIRES PIEZOELECTRIC TRANSDUCER

The two-wires piezoelectric transducer is a second alternative proposed for the current measure. It consists of using the well known property of the creation of a magnetic force when a current is driven for two parallel wires when the distance between them is little.

If the current in both conductors is driven in the same direction, the appeared force will tend to approach the conductors. On contrary, if the current in one conductor is opposite to the current in the other one, the force will tend to separate both conductors. Figure 6 shows a schematic of the first case.

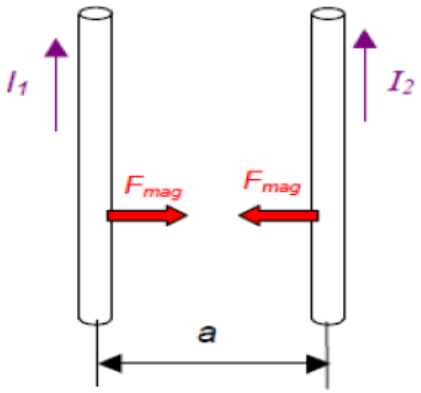

Fig. 6 : Force appearing when a current is driven in two parallel conductors

VIII. PROTOTYPE OF A TWO-WIRES PIEZOELECTRIC CURRENT SENSOR

A. *Prototype construction*

Two types of construction have to be evaluated, depending upon, if both currents will drive in the same sense or on contrary senses. In the first case, the appeared forces will always be in compression, while in the second case the forces will be tensile. Here is discussed a prototype with compressive forces. This type of device has the advantage in front of the tensile-type that the decoupling between piezoelectric discs and the conductors does not occur and the mechanical requirements are lower.

B. *Prototype with two parallel currents*

The prototype, shown in Figure 7, consists of two piezoelectric rings of PZT-5 connected in parallel. The current arrives to the sensor and in an upper and lower copper electrode. In this way two parallel currents appear in both sides of the piezoelectric sensor and so a compressive force. The path of the current is closed in the opposite end. The external electrodes of the sandwich are connected to ground and the middle electrode provides the generated output voltage. Both copper electrodes have constructed to provide a necessary stiffness to the sandwich (quasi-blocking measurement). The sensor is initially fixed together with the electrodes by using a screw passing through the internal hole.

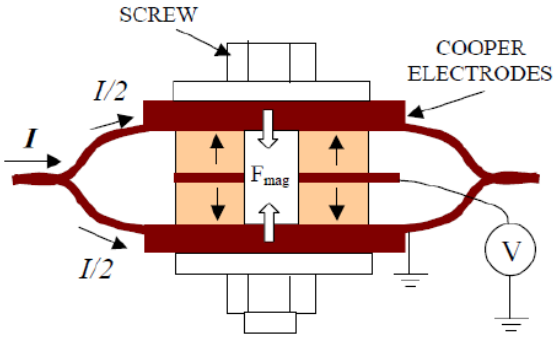

Fig. 7 : Two-wire piezoelectric current sensor

IX. SOFTWARE DESIGN AND ANALYSIS

The basic principle is: Firstly, the parameters, such as the primary input current to the system, supply frequency and time period is defined. Next for calculation of force other parameters, such as permeability length of conductor material and distance between two conductors is defined likewiseMATLAB based Algorithm is developed for system simulation. The calculation process diagram of software is shown in figure 8.

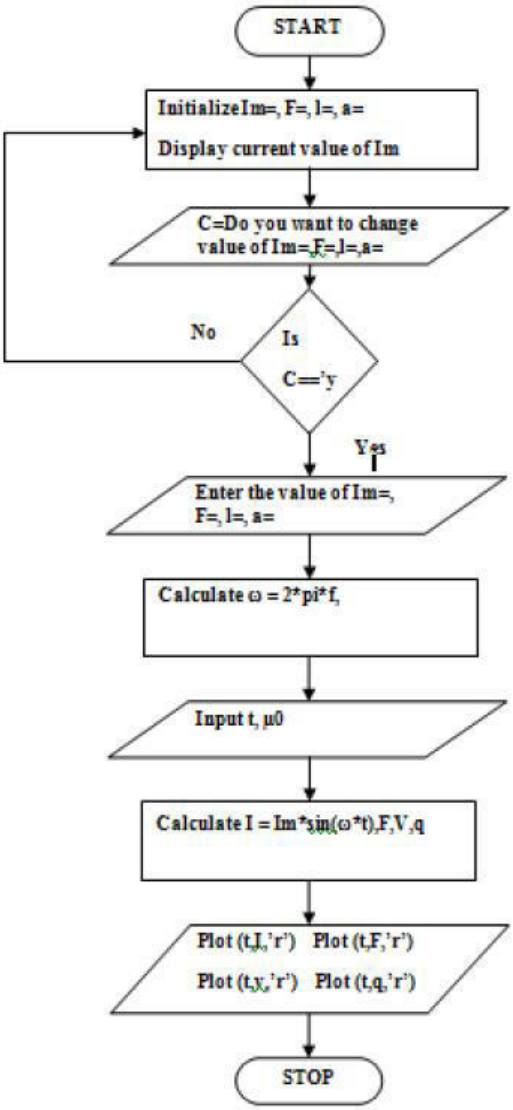

Fig. 8 : The Flowchart of system algorithm

A. *Performance test*

In the process of testing piezoelectric current sensor, firstly we have to decide appropriate piezoelectric material which is suitable for better performance of the system which has to be simulated and verified in MATLAB environment and for the same we developed an algorithm such that from which we can able to decide exact material requirement for piezoelectric current sensor by verifying performance characteristics of the piezoelectric material in MATLAB/SIMULINK.

B. *Piezoelectric material characteristics*

The simulation results exhibit that there is variation in response for each different piezoelectric material depend up on material properties such as, piezoelectric charge constants and piezoelectric voltage constants.

The results illustrate the measured force in the piezoelectric sensor when an input current of 200A is driven, the voltage response of different piezoelectric material, the charge response of three different material and finally secondary current response under an primary input current of 200A. Likewise other than this we can able to prepare best piezoelectric combination for different needs of power system operation.

Traditional design flow to implement the new approach has problems of hidden mistakes, material wastage due to different experiment for testing the prototype and economical viability. To overcome this problem, system is firstly programmed against required simulation results and verification in MATLAB environment. The present paper also proposes a novel approach to realize piezoelectric current sensor system. In which designs system from MATLAB programmed and generate hardware description parameter after the verification without need of hardware program manually, this approach has the advantages in the flexibility and economically efficient system implement. The approach is suitable for any system which can be described in MATLAB first and will be applied widely. From this simulation results we come to know that best suitable material requirement with appropriate dimensions and after that we can able to design prompt hardware structure that guarantees very stable operation.

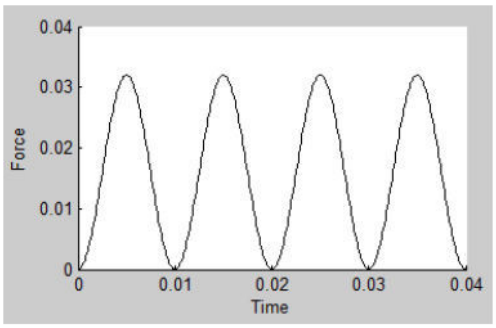

Fig. 9 : The magnitude of generated force under a primary current of 200A.

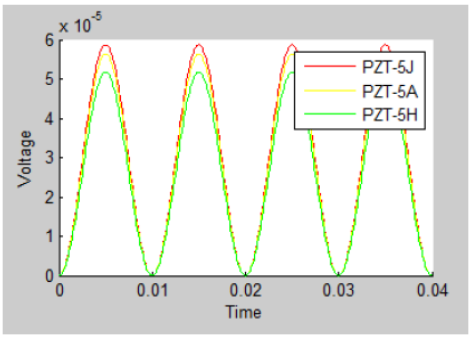

Fig. 10 : The voltage response of different piezoelectric material under the force generated by 200A primary current.

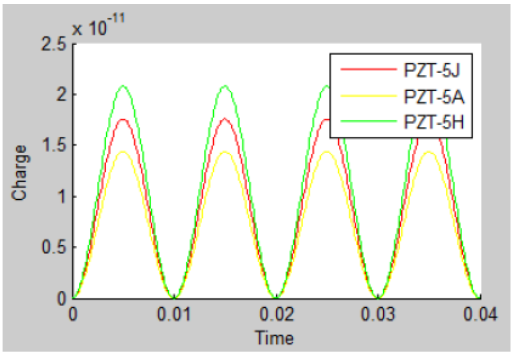

Fig. 11 : The charge response of different piezoelectric material under the force generated by 200A primary current.

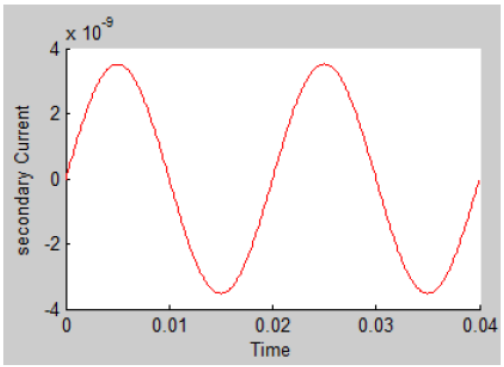

Fig. 12 : The secondary current response of piezoelectric sensor under an electrical current of 200A.

X. CONCLUSION

Two configurations of piezoelectric current transformers have been discussed. The electromagnetic-piezoelectric transducer configuration has core saturation problems, due to the use of a magnetic core for generating the electrical signal. In particular, their weight is not significantly reduced compared to the electromagnetic transformers, they can saturate, in spite of the gap used for the sensor placement and hysteresis may appear.

On the other hand, the Two-wire piezoelectric transducer is a more reliable alternative for measuring current. It reduces in a 100% the magnetic core use, and so core saturation problems of it.

The Two-wire piezoelectric transducer presented represents only the first successful step in the research in the field of piezoelectric current transducer. In the future, it is necessary to analyze the mechanical structure that guarantees a very stable operation.

Another important effect to be analyzed corresponds to the effects of the temperature in the measurements. Ceramic materials are pyroelectrics and

then they stability in front the temperature is very low. The temperature reached by the wire when currents of the order of 100A or more is driven can be very important and thus the effect in the behavior of the sensor. A countermeasure to this consists in the use of piezoelectric materials with a good thermal stability, such as quartz.

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CMOS Inverter Based Low-Power Full-Adder and Decoder

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Abstract - CMOS inverter based Low-power full-adder and 2-to-4 Line Decoderis presented. This full-adder and 2-to-4 Line Decoder is comprised of inverters. Universal gates such as NOR, NAND and MAJORITY-NOT gates are implemented with a set of inverters and non-conventional implementation of them.The design performance is evaluated by comparing it with the conventional design of the Static logic Gates and Full adderand 2-to-4 line Decoder The simulation results are analyzed with technology parameters to show the technology independence of the design. Proposed CMOS inverter based Low-power full-adder and 2-to-4 line Decoderis better suitable for the low power VLSI applications.

Keywords - *CMOS VLSI Design, Full adder cell, Low Power, Power –Delay Product,MOSCAPMajority-not gate,2-to-4 line Decoder.*

I. INTRODUCTION

Arithmetic operations are widely used in many VLSI applications. Addition is a very basic operation in arithmetic Proposed CMOS inverter based Low-power full-adder is introduced which only uses inverters and transmission gates. This full-adder has a simple structure but it operates very well and results in remarkable advances in reducing power in comparison to other well-known designs. This reduction is due to simple structure, reduced number of transistors and the lowering in switching activities [7]. Again, it is worth mentioning that in the proposed design only a few inverters and pass gates have been used, thus the number of transistors have been decreased. The 1-bit Full Adder cell is the building block of an arithmetic unit of a system. Thus, its performance directly affects the performance of the whole system. In other words, increasing the performance of a 1-bit Full Adder cell is very critical for increasing the overall performance of the system.

Addition is a very basic operation in arithmetic. Subtraction, multiplication, division and address calculation are some of the well-known operations based on addition. These operations are widely used in many VLSI applications, since the full-adder cell is the building block of the binary adder, enhancing the performance of the 1-bit full-adder is a significant goal and has attracted much attention. Two important attributes of all digital circuits reducing power consumption and increasing speed. CMOS inverter based low-power full-adder. This full-adder is comprised of inverters. Universal gates such as NOR, NAND and MAJORITY-NOT gates are implemented with a set of inverters. They enjoy low-power dissipation due to their transistor counts. To implement NAND Gate it is just enough to use high-V_{th} NMOS and low-V_{th} PMOS. For implementing NOR gate, high-V_{th} PMOS and low-V_{th} NMOS have been used and finally in order to have MAJORITY-NOT Function both transistors are replaced with high-Vth transistors..

The circuit for implementing the universal gates is illustrated in Fig. 6. Because of just two transistors in Fig. 5 the supply voltage can be reduced .In this situation $P_{short\text{-}circuit}$ is eliminated due to Eq. (2),and because of low voltage scaling, $P_{dynamic}$ is reduced in a quadratic manner .So the average power dissipation is lower than conventional CMOS gates. Although lowering supply voltage and modifying the threshold voltage results in decreasing the power consumption , modifying V_{th} and reducing supply voltage have direct influence on latency of the circuit. To implement NAND Gate with Fig. 6 it is just enough to use high-V_{th} NMOS and low-V_{th} PMOS. For implementing NOR gate, high-V_{th} PMOS and low-V_{th} NMOS have been used and finally in order to have MAJORITY-NOT Function both transistors are replaced with high-V_{th} transistors . Using high-threshold voltage transistors and low-threshold voltage transistors in addition to normal-threshold transistors have been accomplished in low-power application ,and many circuits have enjoyed this technique in low-power design. Multi-threshold CMOS(MTCMOS)circuits and dual-V_{th} techniques use high-V_{th} transistors to eliminate and reduce the leakage current through a transistor ,thereby decreasing leakage power consumption while maintaining performance. So reducing the leakage power and the propagation delay time to design energy efficient high speed circuit with

low-power-delay product is achievable by using modified threshold voltage transistor in circuit path [5].

The total power dissipated in a generic digital CMOS gate is given by

$$P_{total} = P_{dynamic} + P_{shortcircuit} + P_{static} = V_{dd} F_{clk} \sum_i V_{i\,swing} C_{i\,load} \alpha_i + V_{dd} \sum_i I_{i\,sc} + V_{dd} I_l \quad (1)$$

Where F_{clk} denotes system clock frequency, $V_{i\ swing}$ is the voltage swing at node i (ideally equal to V_{dd}), $C_{i\ load}$ is the load capacitance at node i, α_i is the activity factor at node i, and $I_{i\ sc}$ and I_l are the short circuit and leakage currents.

In classical CMOS inverters, when both transistors turn on at the same time, power consumption will be increased .If $P_{short\text{-}circuit}$ can be eliminated, the power dissipation will be decreased by a remarkable amount [4]. This can occur when both of transistors are not able to be on at the same time. There are three major components of power dissipation, $P_{dynamic}$, $P_{short\text{-}circuit}$, P_{static}.

- $P_{dynamic}$ denotes the switching component of power where, V_{DD} is the power supply voltage, f_{clk} is the system clock frequency, and V_{swing} is the voltage swing of the output, C_{iload} is the output load capacitance at node i, and α_i is the transmission activity factor at node i.
- $P_{short\text{-}circuit}$ represent the short-circuit power, which results from I_{isc} following from power supply to ground at node i, which is negligible due to its small value in our circuits.
- P_{static} denotes the leakage power, which is derived from leakage current Il which is due to reverse-biased junction leakage current and subthreshold leakage current.

$$V_{dd} < |V_{tp}| + V_{tn} \quad (2)$$

Where V_{tp} and V_{tn} are threshold voltages for PMOS and NMOS transistors, respectively Threshold voltage is a voltage at which channel formation occurs in a metal–oxide–semiconductor field- effect transistor (MOSFET).

Proposed CMOS inverter based Low-power full-adder. This full-adder is comprised of inverters [1]. Universal MAJORITY-NOT gates are implemented with a set of inverters In this approach the time consuming XOR gates are eliminated by the technique used in designing MAJORITY-NOT function. They enjoy low-power dissipation due to their transistor counts.

In this paper, Proposed CMOS inverter based Low-power full-adder and . 2-to-4 Line Decoder is Presented. This full-adder is comprised of inverters [1]. Universal MAJORITY-NOT gates are implemented with a set of inverters In this approach the time consuming XOR gates are eliminated by the technique used in designing MAJORITY-NOT function. They enjoy low-power dissipation due to their transistor counts.The design is compared with the conventional design of Static logic Gates and Full adder and . 2-to-4 line Decoder. The Low Power Static logic Gates and Proposed CMOS inverter based Low-power full-adderand . 2-to-4 Line Decoderand the conventional designs are simulated and analyzed at 90nm technologies to show the technology independence. The designs are observed keeping the power dissipation, delay and area as parameters.

This paper is organized as follows: the next section describes about the design of Low Power Static logic Gates andProposed CMOS inverter based Low-power full-adderand . 2-to-4 line Decoderalong with the conventional Static logic Gates and adder. In the next section the designs are simulated and simulation data is analyzed followed by conclusions and references.

II. STATIC LOGIC GATES ,ADDER AND DECODER DESIGN

A logic gate is an elementary building block of a digital circuit . Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions low(0) or high(1), represented by different voltage levels. Static logic Gates are NAND,NOR,NOT. The NAND gate operates as an AND gate followed by a NOT gate. A Low output results only if both the inputs to the gate are High. If one or both inputs are Low, a High output results. NAND gates can also be made with more than two inputs, yielding an output of Low if all of the inputs are High, and an output of High if any of the inputs is Low. These kinds of gates therefore operate as n-ary operators instead of a simple binary operator.The NORgate is a combination OR gate followed by an inverter. A High output (1) results if both the inputs to the gate are Low (0). If one or both input is High (1), a Low output (0) results. NOR is the result of the negation of the OR operator. NOR is a functionally complete operation—combinations of NOR gates can be combined to generate any other logical function. A logical inverter, sometimes called a NOT gate to differentiate it from other types of electronic inverter devices, has only one input. It reverses the logic state. The CMOS1-bit full adder cell has 28 transistors. The CMOS structure combines PMOS pull-up and NMOS pull down networks to produce considered outputs. A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information

can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.As its name indicates, a decoder is a circuit component that decodes an input code. Given a binary code of n-bits, a decoder will tell which code is this out of the 2n possible codes Thus, a decoder has n- inputs and 2n outputs. Each of the 2n outputs corresponds to one ofthe possible 2n input combinations.CMOS2-to-4 Line Decoder is Designed using CMOS NAND and NOT gates

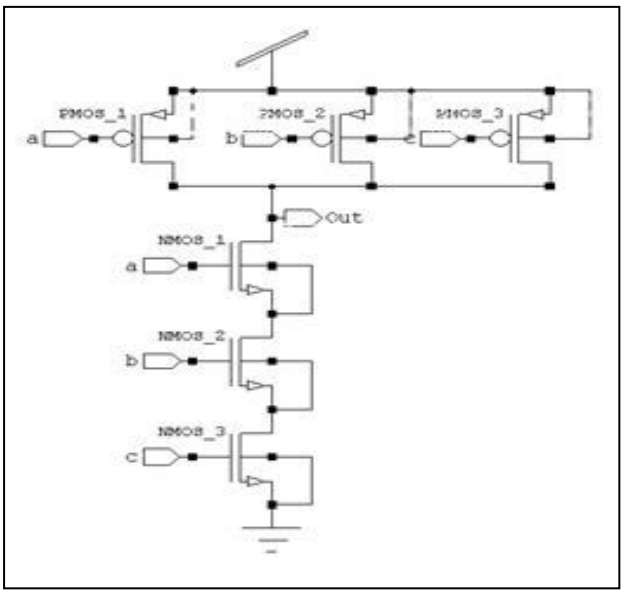

Fig. 1 : Conventional NAND Logic Gate

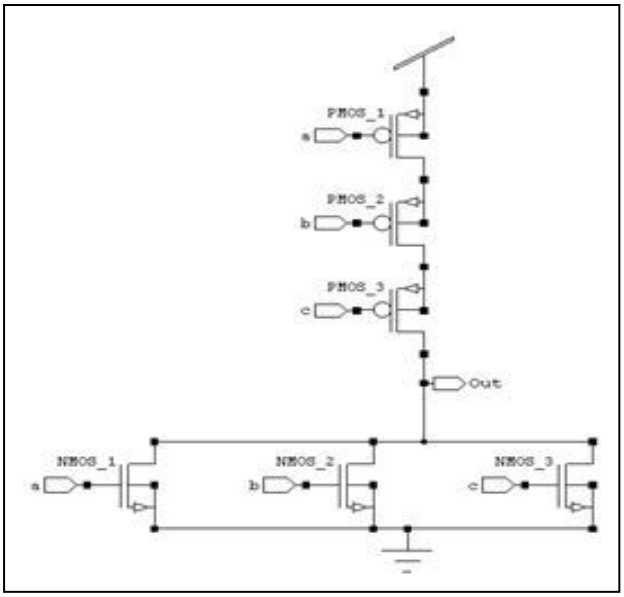

Fig. 2 : Conventional NOR Logic Gate

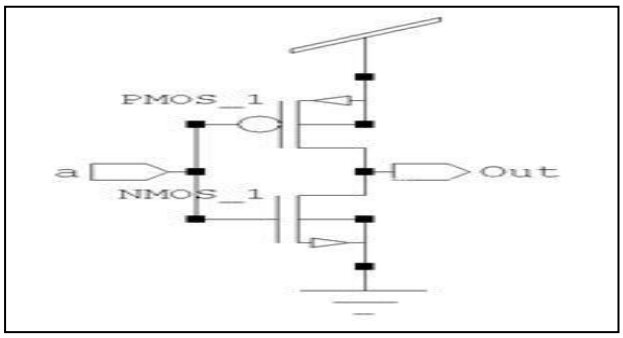

Fig. 3 : Conventional NOT Logic Gate

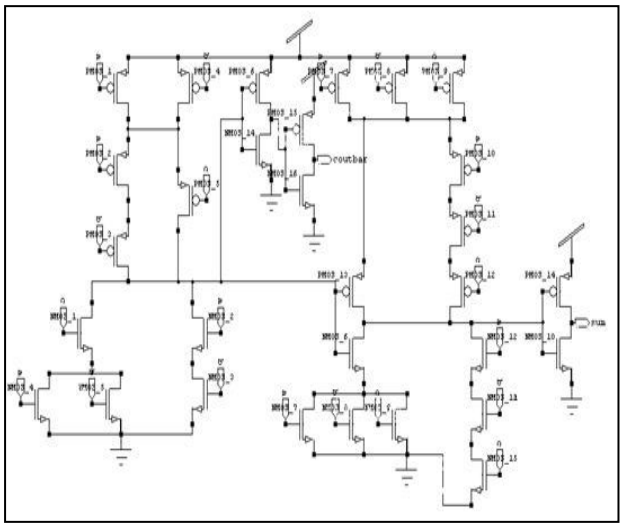

Fig. 4 : Conventional CMOS full adder

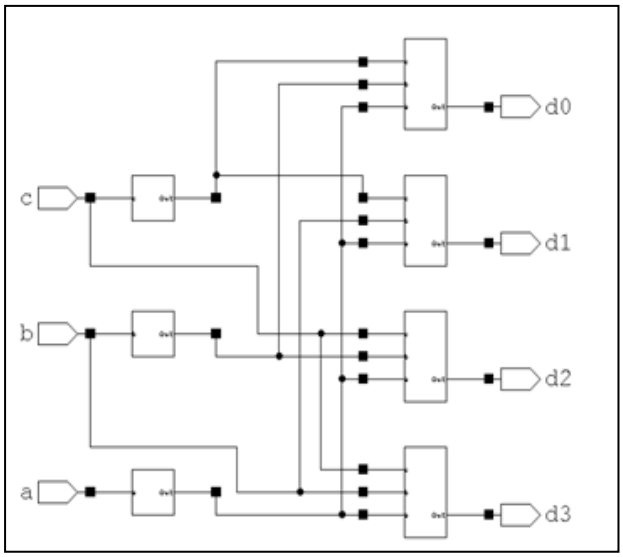

Fig. 5 : Conventional 2-to-4 Line Decoder

The Majority function is a logic circuit that performs as a majority vote to determine the output of the circuits [8]. This function has only odd numbers of

input. Its output is equal to '1' when the number of inputs logic '1' is more than logic '0'. This kind of majority gate is created with input capacitors and a static CMOS inverter.

To implement NAND Gate with Fig. 6it is just enough to use high-V_{th} NMOS and low-V_{th} PMOS. For NAND function, when three inputs (A, B, C) are all '1', output should be '0' otherwise output should be '1'.For implementing NOR gate, high-V_{th} PMOS and low-V_{th} NMOS have been used. For NOR function if there is one input that is '1', output should be '0' otherwise output should be '1'.

Proposed CMOS inverter based Low-power full-adder. The carry output is equal to majority of inputs. Here C_{out} is implemented with a MAJORITY-NOT gate. The six states of the inputs ,the sum output is the reversed of carry output. The two other states can be implemented with a NOR and a NAND gate. When all three inputs of the full-adder are logic zero, the sum output will be logic zero. Thus, a NOR gate can be used to obtain the respective output [6].When the three inputs are logic one, the sum output will be logic one and this output can be detected with a NAND gate. Finally when the three inputs are in the other six states, both of the output transistor, the MN1 and the MP1are off and as was cited, in these six states the sum output of the full-adder is equal to the Cout . In the all-0-state the output of NOR gate is 1 and the MN1 transistor is on .As a result ,the sum output is connected to the Gnd. The all-1-state is detected with the NAND gate .Only in this state the output of this gate is 0 and the MP1 is on which connects the sum output to the power supply. The NAND, NOR and MAJORITY-NOT gates used in this circuit have a similar structure .All of them are based on an inverter. An inverter can implement NOR function if the output is low when the algebraic sum of inputs becomes greater than or equal to logical 1[3]. Identical inverter can implement the NAND gate if the output is low only when algebraic sum of inputs is equal to logical 3. And finally MAJORITY-NOT gate is implemented with an inverter that is low when the algebraic sum of inputs is greater than logical 2. Sum is different in merely two places with Majority not function when inputs are 000 or 111. The value of these two functions are not equal at A=B=C= '0' and A=B=C= '1'. Therefore, we correct these two states by using a pMOS and an nMOS transistor. These transistors must be arranged in such a way that ensures the correctness of the circuit. Three capacitors are used to generate the Carry (majority not function) output. In six mid-states of the Sum output is equal to Carry (majority not function) and the MP1 and MN1 transistors are off. But in all one input state and all zero input state the Sum is obtained by the NAND and NOR gates, respectively. In order to design circuit operations in the given state one nMOS and one pMOS pass transistor are added to the circuit.

Proposed CMOS Inverter Based Low-Power Full-Adder is Designed using MAJORITY-NOT gates. Proposed Low-Power 2-to-4 Line Decoder is Designed using CMOS Inverter Based NAND and MAJORITY-NOT gates

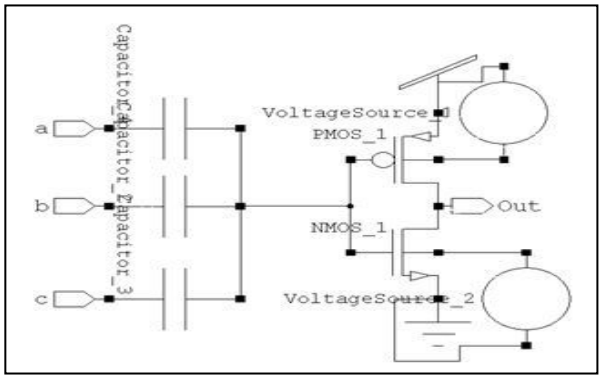

Fig. 6 : Low Power NAND,NOR,MAJORITY-NOT Logic Gate

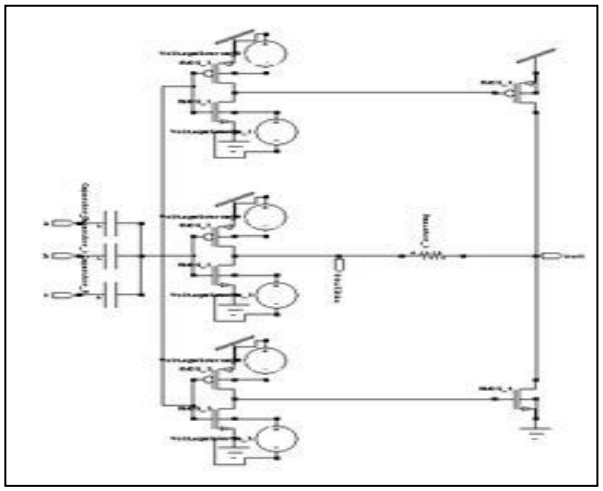

Fig. 7: Proposed CMOS inverter based Low-power full-adder.

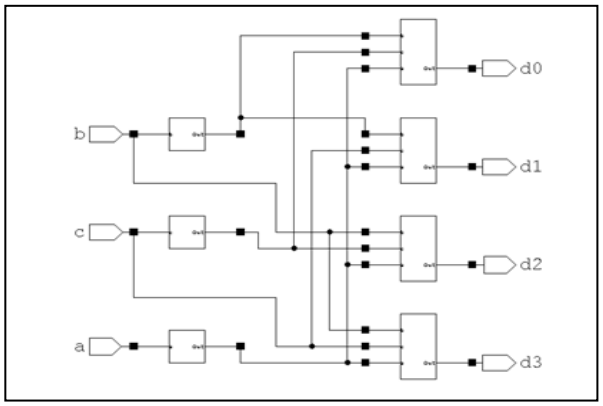

Fig. 8 : Proposed CMOS inverter based Low-power 2-to-4 Line Decoder

III. SIMULATION AND ANALYSIS

In low power applications area, power consumption, and delay introduced by the device are the main technological aspects to prefer a design over the other contending designs.Three input NAND, Three input NOR, NOT Gate based on CMOS and Three input NAND, NOR, MAJORITY-NOT function Gate with capacitorsbased on CMOS Inverter are simulated using T Spice in 90nm standard CMOS technologies .The transistor sizing in subthreshold may have affected the power consumption. Here, we consider equal *(W/L)* ratio of 1 is for all nMOS and pMOS transistors The simulations were performed at different supply voltages (ranging from1.4V to 1.1V).. From simulation result it is shown that forThree input NAND, Three input NOR, NOT Gate based on CMOS and Three input NAND, NOR, MAJORITY-NOT function Gate with capacitorsbased on CMOS Inverter power dissipation and power delay product decrease as supply voltage decrease**.**Low-power full-adder is successfully implemented using CMOS and CMOS Inverter are simulated using TSpice in 90nm standard CMOS technologies .The transistor sizing in subthreshold may have affected the power consumption. Here, we consider equal (W/L) ratio of 1 is for all nMOS and pMOS transistors The simulations were performed at different supply voltages (ranging from1.4V to 1.1V).and. Simulation results for full-adder shows that power dissipation and power delay product decrease as supply voltage decrease for both CMOS and CMOS Inverter.

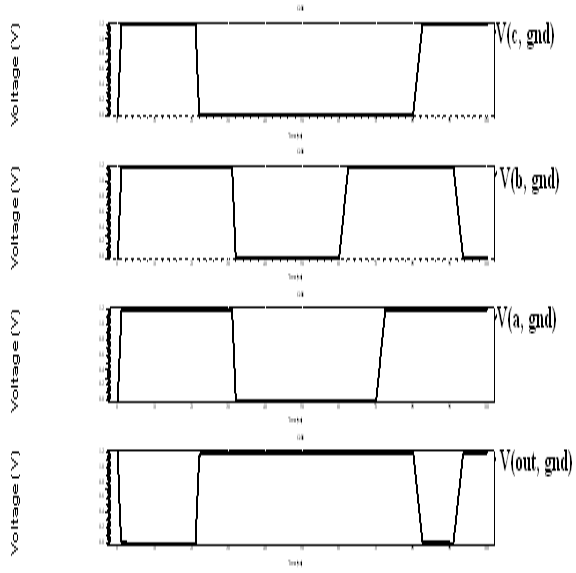

Fig. 9 : Output waveform of the Low Power NAND Logic Gate

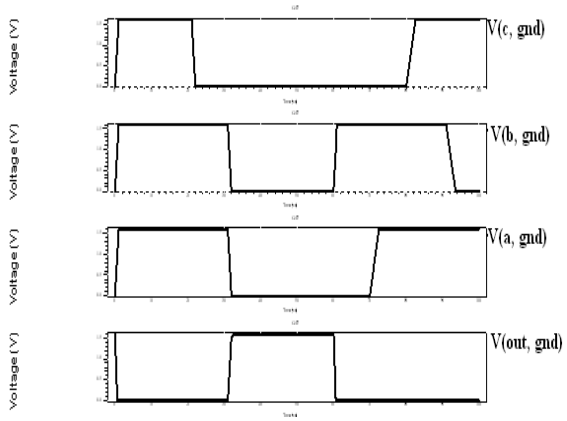

Fig. 10 : Output waveform of the Low Power NOR Logic Gate

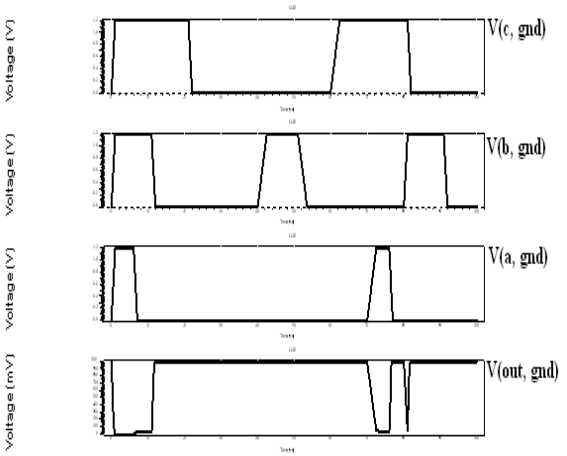

Fig. 11 : Output waveform of the Low Power *MAJORITY-NOT* Logic Gate

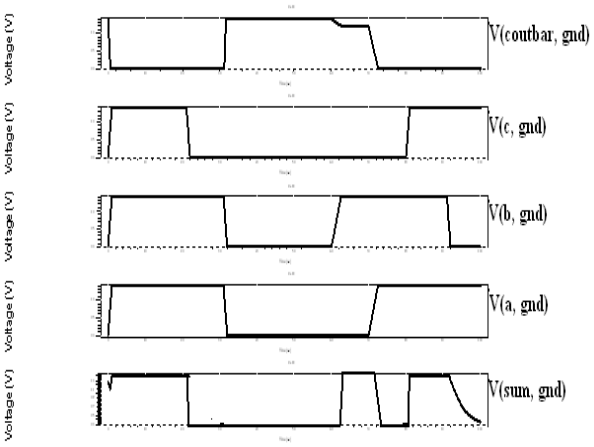

Fig. 12 : Output waveform of the Proposed CMOS inverter based Low-power full-adder.

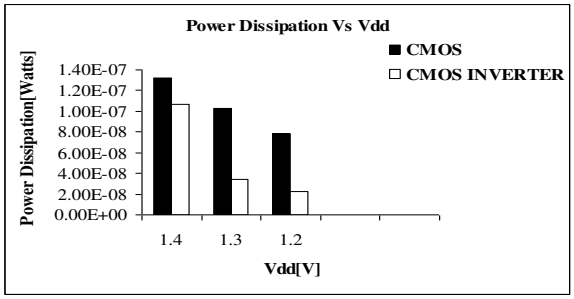

Fig. 13: Power dissipation comparison of NAND Logic Gate at various supply voltages (V)in 90nm technology

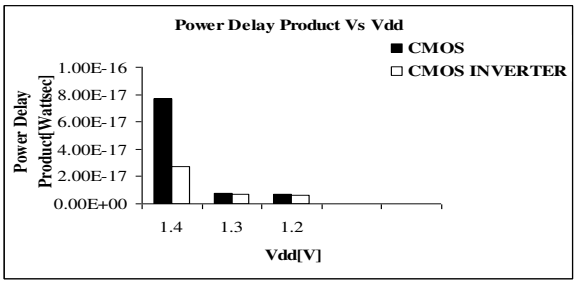

Fig. 14: Power delay comparison of NAND Logic Gate at various supply voltages (V)in 90nm technology

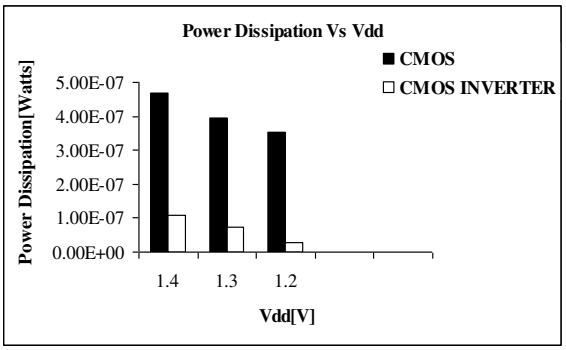

Fig. 15: Power dissipation comparison of NOR Logic Gate at various supply voltages (V)in 90nm technology

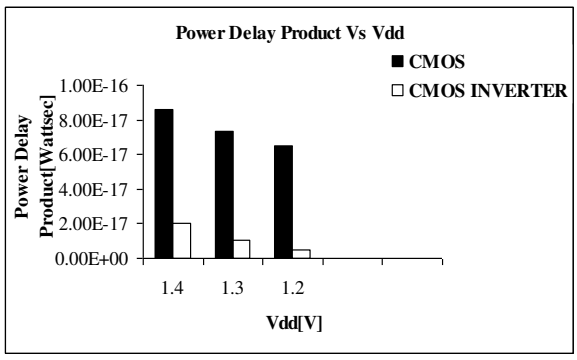

Fig. 16: Power delay comparison of NOR Logic Gate at various supply voltages (V)in 90nm technology

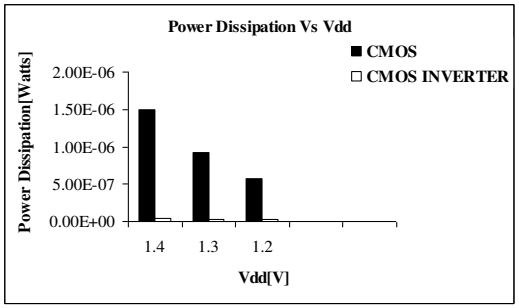

Fig. 17 : Power dissipationcomparison of MAJORITY-NOT Logic Gate at various supply voltages (V)in 90nm technology

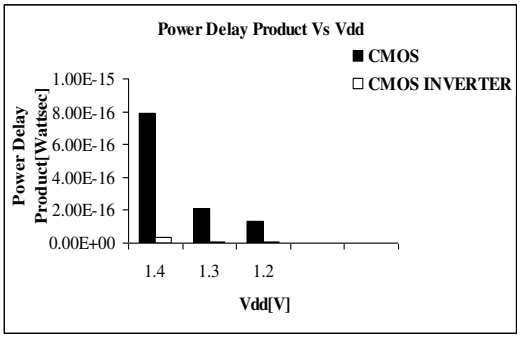

Fig.18: Power delaycomparison of MAJORITY-NOT Logic Gate at various supply voltages (V)in 90nm technology

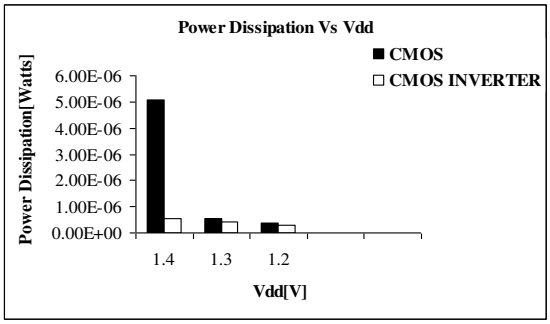

Fig. 19 : Power dissipationcomparison of Proposed CMOS inverter based Low-power full-adder. at various supply voltages (V)in 90nm technology

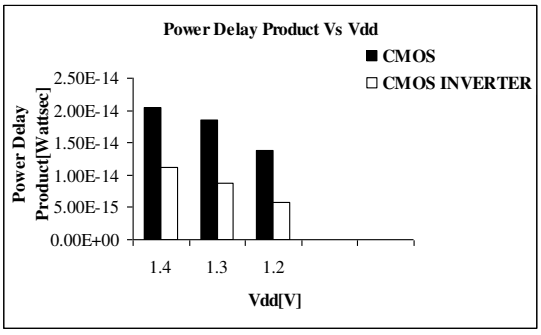

Fig. 20: Power delaycomparison of Proposed CMOS inverter based Low-power full-adderat various supply voltages (V)in 90nm technology

TABLE I

Power dissipation at various supply voltages (V)in 65nm technology

Vdd (V)	Power Delay Product (Wattsec)	
	1-Bit Full Adder	
	CMOS	CMOS Inverter
1.4	20.45E-15	11.17E-15
1.3	18.61E-15	8.72E-15
1.2	13.86E-15	5.77E-15

TABLE II

Power delay Product at various supply voltages (V)in 65nm technology

Vdd (V)	Power Dissipation (Watt)	
	1-Bit Full Adder	
	CMOS	Proposed CMOS Inverter
1.4	5.074E-006	5.11E-007
1.3	5.477E-007	4.89E-008
1.2	3.937E-007	1.55E-008

TABLE III

Power dissipation at various supply voltages (V)in 65nm technology

Vdd (V)	Power Dissipation (Watt)	
	2-to-4 Line Decoder	
	CMOS	Proposed Low Power
1.4	1.07E-006	3.54E-007
1.3	1.22E-006	4.75E-007
1.2	1.43E-006	5.84E-008

Power dissipation and Power delay product comparison graph of Three input NAND Gate based on CMOS and Three inputNAND Gate with capacitors based on CMOS Inverter at different supply voltages are Shown in 13 and 14. Here figure 13 and figure 14 depicted that Three input NAND Gate with capacitors based on CMOS Inverter reduces 70% power dissipation and 12% power delay product than Three input NAND Gate based on CMOS at supply voltage of 1.2V. Power dissipation and Power delay product comparison graph of Three input NOR Gate based on CMOS and Three inputNOR Gate with capacitors based on CMOS Inverterat different supply voltages are Shown in 15 and 16.Here figure 15 and figure 16 depicted that three input NOR Gate with capacitors based on CMOS Inverter reduces 92% power dissipation and 92% power delay product than Three input NOR Gate based on CMOS at supply voltage of 1.2V. Power dissipation and Power delay product comparison graph ofNOT Gate based on CMOS and Three input MAJORITY-NOT Gate with capacitors based on CMOS Inverter at different supply voltages are Shown in17 and 18. Here figure 17 and figure 18 depicted that Three input MAJORITY-NOT Gate with capacitors based on CMOS Inverter reduces 95% power dissipation and 96% power delay product than NOT Gate based on CMOS at supply voltage of 1.2V. Power dissipation and Power delay product comparison graph of 1-bit full adder based on CMOS and Proposed CMOS inverter based Low-power full-adder.at different supply voltages are Shown in 19and 20. Here figure 19 and figure 20 depicted that Proposed CMOS inverter based Low-power full-adder.reduces 30% power dissipation and58% power delay product than 1-bit full adder based on CMOS at supply voltage of 1.2V. Proposed CMOS inverter based Low-power. 2-to-4 Line Decoderhas small power dissipation and power delay productas compared to CMOS2-to-4 Line Decoderat supply voltage of 1.2V

IV. CONCLUSION

The simulation results are analyzed with technology parameters to show the technology independence of the designProposed CMOS inverter based Low-power full-adder and 2-to-4 Line Decoder.This full-adder is comprised of inverters. Universal MAJORITY-NOT gates are implemented with a set of inverters In this approach the time consuming XOR gates are eliminated by thetechnique used in designing MAJORITY-NOT function. They enjoy low-power dissipation due to their transistor counts. Proposed CMOS inverter based Low-power full-adder and 2-to-4 Line Decoder.has been presented in this paper and the presented technique has small power dissipation and power delay product as compared to 1-bit Full adder based on CMOS and CMOS2-to-4 Line Decoder. Simulations based on T Spice 90nm CMOS technology. The simulations were performed at different supply voltages.

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Study on Peak to Average Power Ratio in OFDM System

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Abstract - High data rate wireless access is demanded by many applications. In any system, high data rate transmission requires high bandwidth. But spectrum becomes scarcer day by day with increase in wireless access and wireless devices. In this case, Orthogonal Division Multiplexing is the best alternative solution. OFDM provides high speed data transmission by using orthogonal channels .It also provides robustness against Inter symbol Interference (ISI) and multipath fading. In spite of these advantages OFDM has a major disadvantage of the Peak-to-Average Power Ratio(PAPR).There are many techniques which are used to reduce PAPR in OFDM system like Amplitude Clipping, Clipping and filtering, Selective mapping, Partial transmit technique, Tone reservation and coding schemes. In this paper, review on different reduction techniques and comparison between these techniques has been given. Bit error is calculated for basic OFDM system. PAPR is also calculated for OFDM system using BPSK modulation by taking different number of subcarriers.

Keywords - *OFDM, PAPR, CCDF, SLM, PTS.*

I. INTRODUCTION

OFDM is one of the many multicarrier modulation techniques, which provides high spectral efficiency, low implementation complexity, less vulnerability to echoes and non – linear distortion. Due to these advantages of the OFDM system, it is vastly used in various communication systems. But the major problem one faces while implementing this system is the high peak – to – average power ratio of this system. A large PAPR increases the complexity of the analog – to – digital and digital – to – analog converter and reduces the efficiency of the radio – frequency (RF) power amplifier. Regulatory and application constraints can be implemented to reduce the peak transmitted power which in turn reduces the range of multi carrier transmission. This leads to the prevention of spectral growth and the transmitter power amplifier is no longer confined to linear region in which it should operate. This has a harmful effect on the battery lifetime. Thus in communication system, it is observed that all the potential benefits of multi carrier transmission can be out - weighed by a high PAPR value. One of the most crucial issues in OFDM is subcarrier allocation amongst the active users [1][2]. The total available bandwidth is firstly subdivided into narrowband channels each having its own sub carrier known as sub carrier and users are subcarriers depends on different criteria. Researchers are investigating different aspects such as joint power control, rate control and scheduling, data rate, type of data traffic, throughput and delay performances, fairness and delay achievements, computational complexity, condition of propagation channel and other important issues are BER and PAPR. High PAPR means the possibility of BER is high due non linear effects in power amplifier are high. In this paper, we are focusing towards different methods of reducing PAPR.

In next sections, OFDM system model, PAPR problem, Methods to reduce PAPR and comparison between different methods is described.

II. OFDM SYSTEM MODEL

In OFDM, an input data symbols are supplied into channel encoder that are mapped onto BPSK/QPSK/QAM constellation. The data symbols are then converted from serial to parallel and using Inverse Fast Fourier Transform (IFFT) to achieve the time domain OFDM symbols [2]. The time domain symbols can be represented as

$$X_n = \text{IFFT}\{X_k\}$$

$$= \frac{1}{N}\sum_{n=0}^{N-1} x_n e^{j2\Pi kn/N} \qquad 0 \le n \le N-1$$

Where, X_k the transmitted symbol on the K-th subcarriers, N is is the number of subcarriers.

Time domain signal is cyclically extended to prevent Inter Symbol Interference (ISI) from the former OFDM symbol using cyclic prefix (CP).

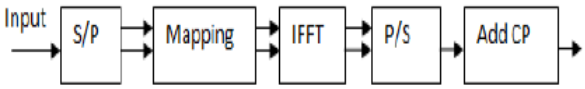

Fig.1: Block Diagram of OFDM System

III. PEAK-TO-AVERAGE-POWER- RATIO AND CCDF

A. *Peak-to-Average-Power- Ratio*

One of the major drawbacks of the OFDM system is high PAPR. OFDM signal consists of many independent modulated subcarriers, which are created the problem of PAPR. It is impossible to send this high peak amplitude signals to the transmitter without reducing peaks [4]. So high peak amplitude signal should be reduced before transmitting. If there are N subcarriers which are in phase then peak power is N time the average power. For sampled signal PAPR is defined as

$$\text{PAPR}=\frac{\max |s_n|^2}{E[|s_n|^2]}$$

where, $E[|s_n|^2]$ is average power of transmitted signal.

$$P(x_k) = \Pr[X = x_k],$$

Where, x_k represents possible values of X.

B. *Cumulative Distribution Function*

The Cumulative Distribution Function (CDF) is one of the most regularly used parameters, which is used to measure the efficiency of any PAPR technique. Normally, the Complementary CDF (CCDF) is used instead of CDF, which helps us to measure the probability that the PAPR of a certain data block exceeds the given threshold. PAPR can take a value in the range that is proportional to number of subcarriers. Probability of symbol with maximal PAPR depends on the number of subcarriers. OFDM symbols with high PAPR have small number of probability with the large number of subcarriers[4]. Therefore, Cumulative distribution function is used to formulation of PAPR probability.

$$F(x) = Pr[X \leq x]$$

In case of discrete distribution CDF can be expressed as

$$F(x) = \int_{-\infty}^{x} f(x)dx$$

$$f(x) = \sum_{k=1}^{K} \delta(x - x_k)P(x_k)$$

where,

Therefore, Cumulative Distribution Function is the probability such that variable X takes a value less than or equal to x.

IV. PAPR REDUCTION TECHNIQUES

Numbers of techniques have been introduced in the literature for reducing Peak to Average Power Ratio. There are two types of techniques signal scrambling and signal distortion techniques. Coding techniques comes under signal scrambling techniques. Other solutions of signal scrambling techniques are Selective Mapping (SLM), block coding, Partial Transmit Sequence (PTS).Signal distortion techniques are signal clipping, Clipping and filtering, Peak Windowing, Peak reduction carrier and companding.

A. *Signal Clipping and filtering*

PAPR is the main drawback in OFDM. With the increase in number of subcarriers PAPR increases due to constructive superposition of subcarriers. High Peak power makes demand on High Power amplifiers, A/D, D/A converters[5]. Due to amplifier's imperfections peaks are distorted non-linearly and inter modulation product occurs. This gives rise to out of band radiation and ICI (Inter Carrier Interference). Clipping is the simple solution for this problem. In this certain threshold is used to limit the amplitude of time domain signal. If the digital OFDM signal is clipped directly then the resulting clipping noise fall in band and cannot be reduced by filtering. To avoid this aliasing problem OFDM symbol is oversampled with the suitable factor. Clipping cause out of band radiation, so filtering is used to control out of band radiation[6][7]. Clipped time sample is given by

$$|\overline{Sn}| = \begin{cases} |Sn| & if\ |Sn| \leq A \\ A & if\ |Sn| \geq A \end{cases}$$

where, A is the clipping level and Sn is the original signal.

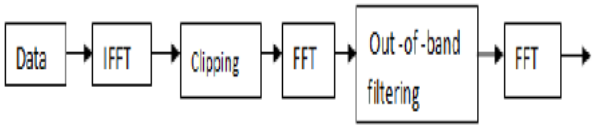

Fig. 2 : Block Diagram OFDM Transmitter with clipping and filtering

B. Peak windowing technique

Peak windowing is also come under the signal distortion technique. In this peak windowing method, different windows like hamming, hanning, cosine and Kaiser may be employed[9]. The basic idea behind this method is to multiply the envelope of OFDM signal with weighting function.

$$s_E(t) = s_E(t) \cdot f(t)$$

Where, $s_E(t) = |s_E(t)|$

The weighting function is given by

$$f(t) = 1 - \sum_{t=t'} \alpha . w(t - t')$$

Where, w(t) is the window function.

t' : denotes the local maxima of the envelope $s_E(t)$

α : Attenuation constant.

A window function is applied to the envelope of the OFDM signal to eliminate the peak amplitude when amplitude of envelope amplitude of the OFDM signal exceeds a threshold.

C. Peak reduction carrier

In this scheme of Peak reduction carrier, to achieve low PAPR, peak reduction carriers are inserted to OFDM symbol. The carriers that are inserted in OFDM symbol are redundant, but can be used for error detection. Phase and amplitude of peak reduction carriers are set to minimalist PAPR. The original information carriers remain unaffected and there is no need of decoding of information on original carriers for the insertion of PRC carriers. Phase, amplitude and position of carriers are used for optimum setting of PRC[10].

D. Selective Mapping

Selective Mapping is one of the signals scrambling scheme. In Selective mapping, set of different carrier signals representing the same information are generated and signal with the lowest PAPR is selected from the set of different signal.SLM provides flexibility as it does not impose any restriction on the modulation technique applied on the subcarriers or their number. SLM reduces PAPR without any signal distortion, but system complexity and computational burden increases. Decrease in number of IFFT blocks can decrease the complexity. By increasing the number of carrier signals, better results can be achieved but side information bits also increases. For detection, receiver needs to know the number of signals that are generated at the transmitter side and this knowledge could be transmitted as side information.SLM becomes highly suitable in most of the practical applications when used in series with the coding schemes such as Golay Complementary Sequence which further reduces the PAPR in OFDM system[11]. Consider an OFDM system with orthogonal subcarriers. A data block is a vector X= $(x_n)N$ which is composed of N complex signal (x_n) and each of them representing modulation symbol transmitted over a sub carrier. X is multiplied element by element with U vector $B_u = (b_{u,n})_N$ composed of N complex numbers $b_{u,n}$ where u ε { 0,1,……,U-1},defined so that $|b_{u,n}|=1$,where |.| denotes modulus operator. Each resulting vector

$Xu = (x_{u,n})_N$ where, $x_{u,n} = b_{(u,n)}.x_n$, produces after IFFT, a corresponding OFDM signal given by

$$s_u(t) = \frac{1}{\sqrt{N}} \sum_{n=0}^{N-1} x_{u,n} e^{j2\Pi n \Delta f t} \qquad 0 \le t \le T$$

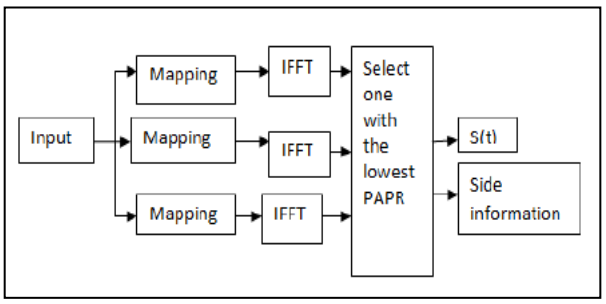

Fig. 3: Block diagram of Selective Mapping

Where, T is the OFDM signal duration and $\Delta f = 1/T$ is the subcarrier spacing. Now, among the modified OFDM blocks, one with the lowest PAPR is selected for transmission and the amount of PAPR reduction of Selective mapping depends on number of phase sequences U and design of phase sequence.

E. Interleaving

Interleaving is the basic technique for PAPR reduction. In interleaving method, the k number of interleavers is used at the transmitter side and these interleavers produces k number of permuted data frames of input data sequence. The frame which has the lowest PAPR of all k frames is selected for transmission. Interleavers can be used either before modulation or after modulation and there is need of side information as identity of corresponding interleavers has to be sent to receiver side [12].

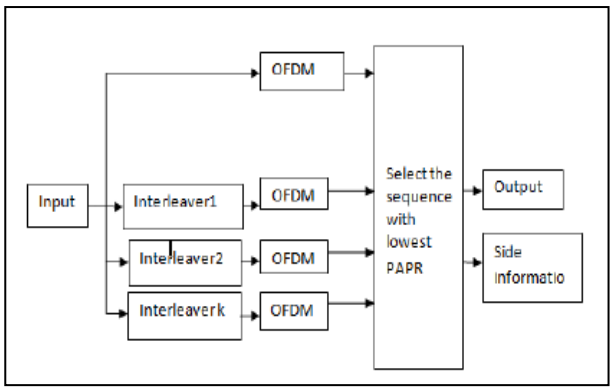

Fig. 4: PAPR Reduction with the interleaving technique

F. Partial Transmit Sequence

Partial transmit sequence is signal scrambling method for PAPR reduction in OFDM system. In this method only that part of data of varying sub-carrier is transmitted, this covers all the information to be sent in a signal. In this method, input data block is partitioned in M disjoint sub blocks where and sub blocks are combined to minimize PAPR in time domain. The L times oversampled time domain signal of input data block which is partitioned in M disjoint sub blocks is obtained by taking the IFFT. These are called partial transmit sequences[13]. Complex phase factors are introduced to combine the PTSs. To minimize the PAPR there is a need to find the set of phase factors. Therefore in PTS method, the main purpose is that the input data frame is sub divided into non overlapping sub blocks and each block is phase shifted by constant factor to reduce PAPR.PTS is a probabilistic method to minimize PAPR and it is better than SLM. It is modified method of PAPR as there is no need to send side information in this method.

G. Combination of different techniques

Two different techniques can be combined to get better results. Two methods from both the group of signal scrambling and signal distortion have been combined [9][12]. Interleaving method is used with W realization, each contains different interleaving matrix and OFDM modulation and IFFT is done. The way with lowest PAPR has been selected from all W realization. The signal with lowest PAPR value has been passed through clipping. The basic need of combining two methods is to obtain signal with lowest PAPR than which is obtained from interleaving method and clipping and filtering alone. In place clipping and filtering peak windowing method have also used for efficiently reducing PAPR. In this method after getting the signal with lowest PAPR from interleaving method, window is applied at the region where high peaks occur and results in smooth signal with minimum PAPR.

V. COMPARISON OF PAPR TECHNIQUES

Different techniques is carefully chosen for minimizing PAPR depending on system requirement, as different techniques has different benefits and disadvantages when parameters like data rate, power, distortion, complexity are considered. Practically, cost analysis and performance analysis can be done before using any PAPR technique.

Table1: Comparison of PAPR techniques

Parameters	Distortion less	Data rate loss	Power Increase
Signal clipping and filtering	No	No	No
Peak Reduction Carrier	Yes	Yes	No
Peak Windowing	No	No	No
Selective Mapping	Yes	Yes	No
Partial Transmit Sequence	Yes	Yes	No
Interleaving	Yes	Yes	No

VI. RESULTS

A. Analysis of BER in OFDM system

Simulation for OFDM system is done in the MATLAB software. OFDM with N=256 subcarriers is evaluated and it employs QPSK modulation. The input data stream is randomly generated. The output variables are stored in MATLAB workspace and BER are stored to draw plots.BER is calculated at the end by using the ratio number of observed errors to the total number of bits transmitted. Performance of Bit error rate is evaluated in Additive White Gaussian Channel for downlink OFDM system. The performance of BER for downlink OFDM system with SNR is calculated and is shown in figure

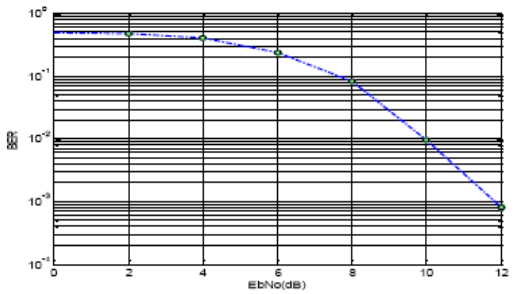

Fig. 5: BER for OFDM system Using QPSK modulation

B. Analysis of PAPR in OFDM system

In OFDM system, PAPR is evaluated by using BPSK modulation. For evaluation of PAPR, N equal to 52 subcarriers are used with IFFT size equal to 64, Number of bits generated are 1000. In figure 6, graph shows that probability of variable X to take value equal to or below x. Then PAPR is evaluated using N=128 subcarriers and IFFT size is 128.Modullation scheme used is BPSK. Figure 7 shows the probability of variable X to take value less than or equal to x with the increase in number of subcarriers.

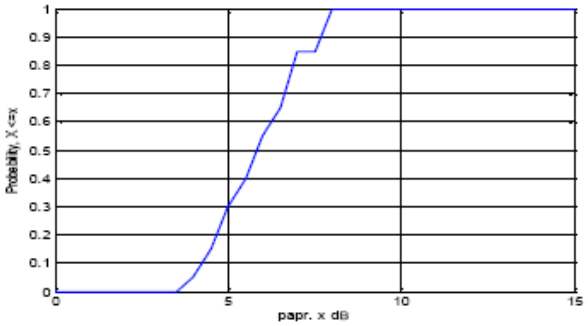

Fig. 6 : Graph for PAPR by using BPSK modulation for OFDM system with N=52.

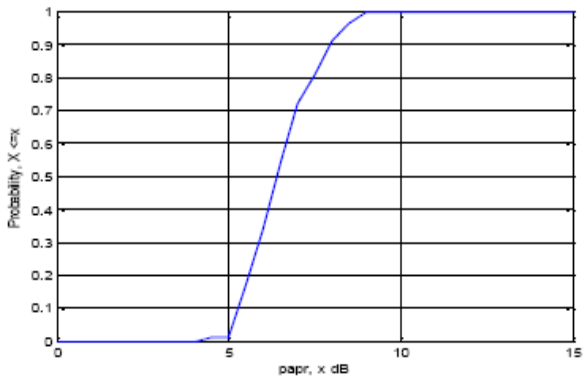

Fig. 7 : Graph for PAPR by using BPSK modulation for OFDM system with N=128

C. PAPR in OFDM system by amplitude clipping

Amplitude clipping technique is applied on OFDM system and plot for PAPR is carried out. Cumulative distribution function gives the probability of measure the probability that the PAPR of a certain data block exceeds the given threshold. PAPR can take a value in the range that is proportional to number of subcarriers. To carry out the PAPR amplitude clipping is employed here and modulation technique used is BPSK. Number of symbols that are used here are 1000 and IFFT size is 128.Certain threshold is set here and peaks above this threshold are clipped and PAPR is evaluated for OFDM system.

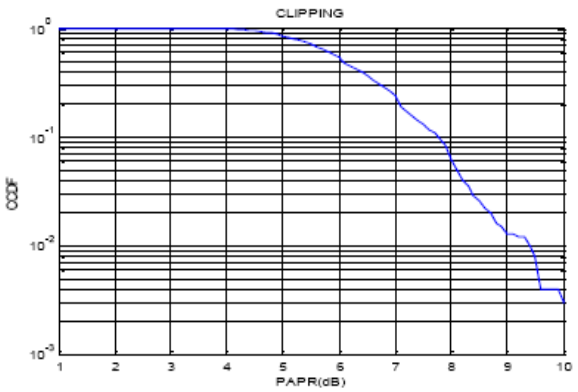

Fig. 8 : PAPR of OFDM system after amplitude clipping

VII. CONCLUSION

OFDM is one of the many multicarrier modulation techniques, which has several advantage of high spectral efficiency, low implementation complexity, less vulnerability to echoes and non – linear distortion. But it has one major drawback of high Peak to average Power Ratio which causes saturation in power amplifier. So there is need to minimize this problem of high PAPR for better performance of OFDM system. Many techniques have been introduced in literature to minimize PAPR such as amplitude clipping and filtering, peak reduction carriers, Selective mapping, Partial transmit sequence. Each method has its own benefits and disadvantages. So for choosing PAPR reduction many factors has to be considered such as data rate, power factor, complexity, need of side information. Therefore, PAPR reduction method is carefully selected depending on the system requirement for better results.

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Aspect Oriented Looming of Smartphones using Object Modelling Approach

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Abstract - Recent years have observed a steep rise in usage of smart phones. earlier the mobile phones are used for a person calling to other person but nowadays, smart phones are used in all aspects such as downloading ringtones, getting any updates and other services such as text messages ,mms ,email ,internet access Short range wireless communication(infrared, Bluetooth). This work aims to model a design of smart phone features and its operations over it... The proposed modeling methodology is based on the principle of object orientation, which allows describing both software and functionalities explicitly. Furthermore, it is illustrated how the well-known object-oriented specification language unified modeling language can be adopted, to provided an adequate formalization of its semantics, to describe structural and behavioral aspects of smart phone database management system related to both logical and physical parts. It is needed to implement the software on the basis of Object Oriented Model developed. Flaw in modeling process can substantially contribute to the development cost and time. The operational efficiency may be affected as well. Therefore special attention should be paid to the correctness of the models that are used at all planning levels and hence Unified Modeling Language (UML) takes its impeccable role.

I. INTRODUCTION

Most of the effort to date in object oriented community has been focused on programming language issues. Objectoriented programming languages are useful in removing restrictions due to the inflexibility of traditional programming languages. In a sense, however, this emphasis is a step backwards for software engineering by focusing excessively on implementation mechanisms, rather than the underlying thought process that they support.

The real pay-off comes from addressing front-end conceptual issues, rather than back-end implementation issues. Design flaws that surface during implementation are most costly to fix than those that are found earlier. Focusing on implementation issues too early restricts the design choices and often leads to inferior product. An object-oriented development approach encourages software developers to work and think in terms of application domain through most of the software engineering lifecycle.

Object-oriented development is a conceptual process independent of programming language until final stages. Object-oriented programming is fundamentally a new way of thinking and not a programming technique. Its greatest benefits come from helping specifiers, developers, and customers express abstracts concepts clearly and communicate them to each other. It can serve as a medium for specification, analysis, documentation and interfacing as well as programming.

Unified Modeling Language (UML) is a standardized general-purpose modeling language in the field of software engineering. UML includes a set of graphical notation techniques to create abstract models of specific systems, referred to as UML model. The Unified Modeling Language (UML) is a graphical language for visualizing, specifying, constructing, and documenting the artifacts of a softwareintensive system. The Unified Modeling Language offers a standard way to write a system's blueprints, including conceptual things such as business processes and system functions as well as concrete things such as programming language statements, database schemas, and reusable software components. UML is officially defined by the Object Management Group (OMG) as the UML metamodel, a Meta- Object Facility metamodel (MOF). Like other MOF-based specifications, UML has allowed software developers to concentrate more on design and architecture.

UML models may be automatically transformed to other representations (e.g. Java) by means of QVT-like transformation languages, supported by the OMG. UML is extensible, offering the following mechanisms forcustomization: profiles and stereotype. The semantics

of extension by profiles have been improved with the UML 1.0 major revision. It is very important to distinguish between the UML model and the set of diagrams of a system. A diagram is a partial graphical representation of a system's model. The model also contains a "semantic backplane" — documentation such as written use cases that drive the model elements and diagrams. UML diagrams represent three different views of a system model:

- Functional requirements view: Emphasizes the functional requirements of the system from the user's point of view. And includes use case diagrams.
- Static structural view: Emphasizes the static structure of the system using objects, attributes, operations and relationships. And includes class diagrams and composite structure diagrams.
- Dynamic behavior view: Emphasizes the dynamic behavior of the system by showing collaborations among objects and changes to the internal states of objects. And includes sequence diagrams, activity diagrams and state machine diagrams.

II. CLASS DIAGRAM

Advanced version of mobilephone is smartphones , which provides advanced connectivity and computing ability than the exisisting phones. Smart phone, the device that has features which are available in a pc, but in a portable format.

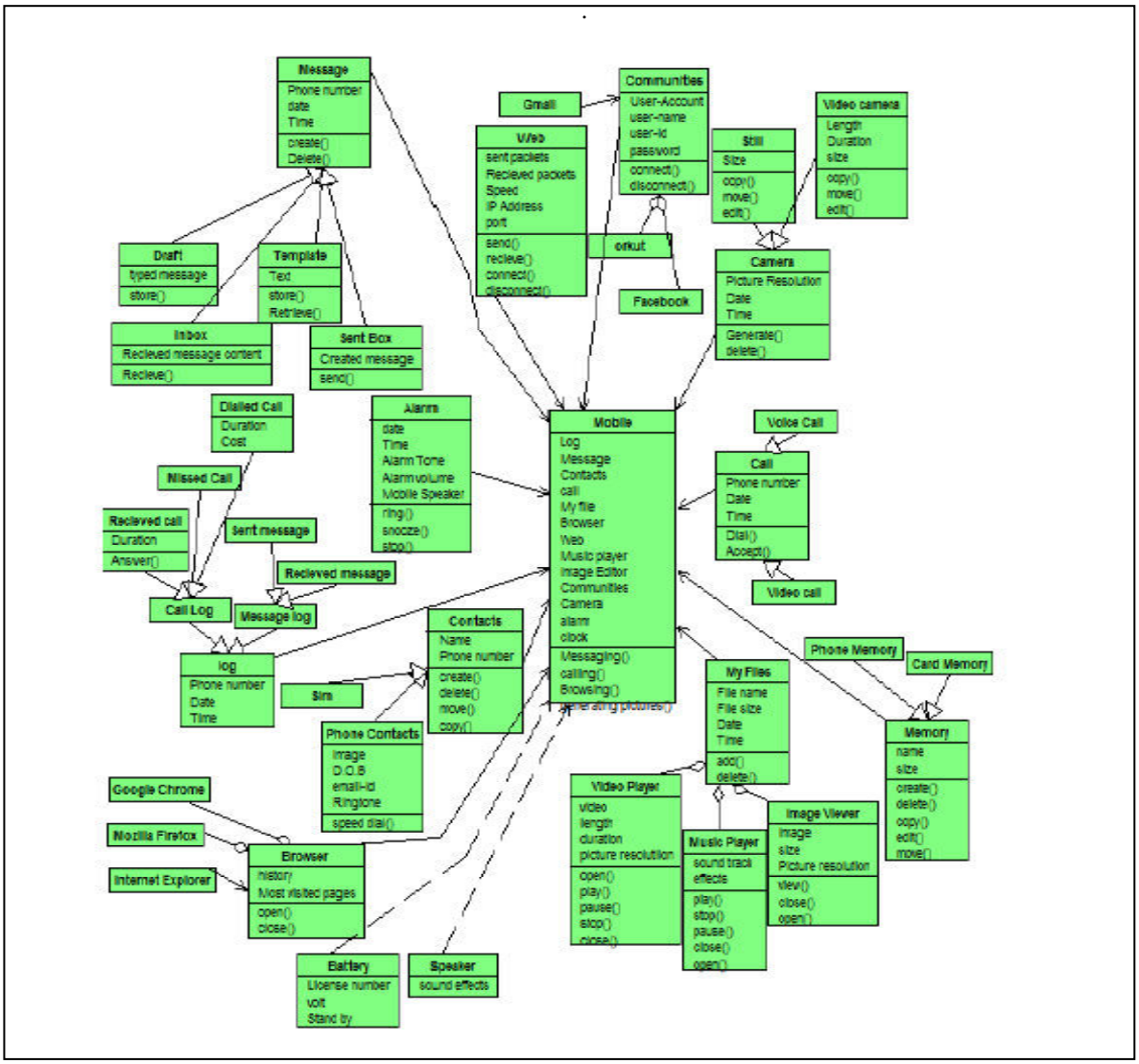


Fig.1 Class Diagram for proposed smart phone

Here are the top features that all smart phone has,

- **Wi-Fi**

No Smart phone is complete without an internet connection which all applications rely on. Wi-Fi connections are easy to find in Café, hotel lounges, College or office campus. Getting connected in seconds.

- **Battery**

Almost all smart phones have some basic features likemp3 player, web browsers, social apps that are evenly supplied with power supply. And can say a heart of a smart phone.

- **RAM**

To support multi-tasking, the device must definitely should have at least 512MB of RAM, to run without any interruption. And the smart phone is well supplied with this memory.

- **Application**

There are thousands of applications which are freely available online and the users are free to use any application that suits his needs.

- **3G technology**

The 3rd generation mobile telecommunication, which supports video calling and a broadband like internet speed makes smart phone more likeable.

- **GPS**

GPS which helps you find directions using latitude and longitude position of map with more accuracy.

The smart phone has the base class as Mobile which has the basic properties and functions that are inherited & used by other classes. The class diagram represents how the class inheritance level and the relationship between each class exist.

Here some classes inherit from the base class and some from the child class. The important classes among them are contacts, log, Message, call and many more. Here, we will discuss about few of the important classes

Contacts : Main important properties are Name and Phone number and has the functions are Create(), delete(), update(), move(). The class then further inherited by sim contacts and phone contacts.

Message: The basic properties for the phone number, Text, Date and Time, which has the same functionality as the Mobile. The message uses few of other classes such as template, by which the message creation is made easier by using the template.

Camera: One of the important multimedia class which are further more used and inherited by video camera and still camera. This class provides the basic functionality for the camera object to use it and has the basic properties such as resolution, date and time.

Alarm: One of its well known functionality for which it is created to always run in the back ground which will be triggered when its time is in match with system time.

Log: The main purpose for log is record all the operation and error which then can be used for bug fixing purpose and advancement purpose. But here we have discussed it for message and call logging which contains complete history about the message and call.

Memory: This class has the important property Size which determines everything else the whole system can hold that are then used for phone and system memory.

III. USE CASE DIAGRAM

Use case diagrams model the functionality of a system using actors and use cases. Use cases are services or functions provided by the system to its users. The components in a use case diagram include:

- **Actors:** Actors represent external entities of the system. These can be people or things that interact with the system that is being modeled. For example, if we are modeling an online store we have many actors that interact with the store functionality. The customer browses the catalog, chooses items to buy, and pays for those items. A stocker will look at the orders and package items for the customer. A billing system will charge the customer's credit card for the amount purchase.
- **Use Cases:** Use cases are functional parts of the system. When we say what an actor does, that's a use case. The customer "browses the catalog", "chooses items to buy", and "pays for the items". These are all use cases. Many actors can share use cases. If we find a use case that is not associated with any actor, this may be a unnecessary functionality.
- **Associations:** Associations are shown between actors and use cases, by drawing a solid line between them. This only represents that and actor uses the use case. There are also two kinds of relationships between use cases:
- **Includes :** Use cases that are associated with actors can be very general. Sometimes they "include" more specific functionality. For example, the "pump gas" use case that is associated with the customer includes three use cases: Choose Gas Type, Fill Tank, and Calculate Total. Includes relationship is represented by dashed arrows that point to the included functionality. Beside the arrow is <<includes>>.

- **Extends :** An extension use case is an insertion to the base use case. For example, some stores may allow for different payment options like credit card, debit card, or cash on delivery. These specific functionalities are extension of the general "pay for items." Extends relationship is represented by dashed arrows that point to the base functionality. Beside the arrow is <<extends>>

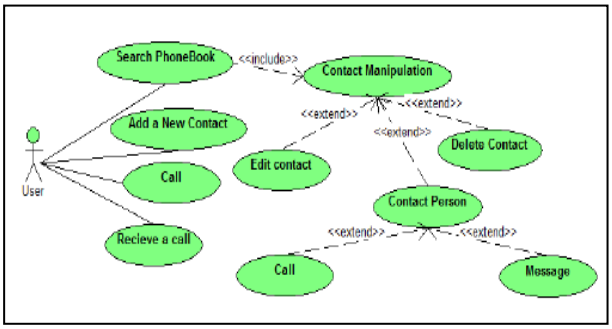
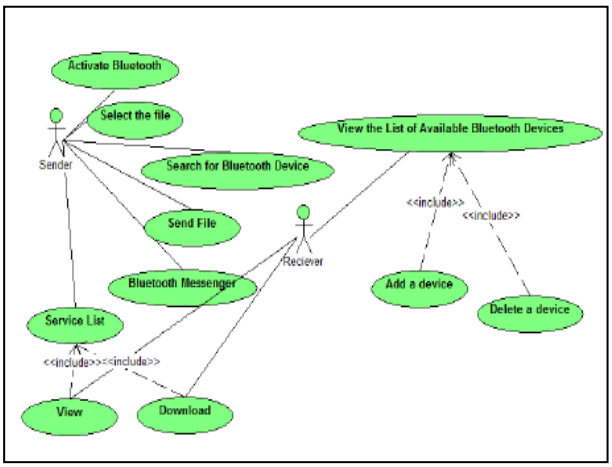


Fig.2 Use case diagram for Contacts

The above use case diagram gives the overview of Contacts in smart phone system .when the user making call, searches for the contact to make a call or manipulate its values. The user can search the contact either by the phone number or its contact name. The user can also directly enter the number by keypad to make a call or to add the number to his/her contact list. The user is able to see the contact details when an incoming call arrives by looking the contact from its contact directory. The user performs more specific tasks editing or deleting the contact from its data dictionary. Along with contact a person through either call or message. In above use case diagram, Editing contact, Deleting Contact and Contacting the persons are different way the user can use the contact information.



¶ Fig 3. Use case diagram for Bluetooth connection establishment

Initially, the user interaction stars with the activating the Bluetooth connection or may be starting with selecting the file for transmitting to another Bluetooth enabled devices. The user can also use bluetooth for making voice call by connecting to wireless headset. The bluetooth provides provides two types of services in filemanager i.e. viewing the list of files in the another system or sending and receiving files from/to another device. The user can view the list of available bluetooth enabled devices from which to a particular device can be enabled, to send or receive files. Here the user can also delete the device from the list of available deveices which are shown in.

IV. INTERACTION DIAGRAM

Interaction diagrams model the behavior of use cases by describing the way groups of objects interact to complete the task. The two kinds of interaction diagrams are sequence and collaboration diagrams. Interaction diagrams are used when you want to model the behavior of several objects in a use case. They demonstrate how the objects collaborate for the behavior. Interaction diagrams do not give a in depth representation of the behavior. Sequence diagrams, collaboration diagrams, or both diagrams can be used to demonstrate the interaction of objects in a use case. Sequence diagrams generally show the sequence of events that occur. Collaboration diagrams demonstrate how objects are statically connected.

The sequence diagram is used primarily to show the interactions between objects in the sequential order that those interactions occur. Much like the class diagram, developers typically think sequence diagrams were meant exclusively for them. However, an organization's business staff can find sequence diagrams useful to communicate how the business currently works by showing how various business objects interact. Besides documenting an organization's current affairs, a business-level sequence diagram can be used as a requirements document to communicate requirements for a future system implementation. During the requirements phase of a project, analysts can take use cases to the next level by providing a more formal level of refinement. When that occurs, use cases are often refined into one or more sequence diagrams. An organization's technical staff can find sequence diagrams useful in documenting how a future system should behave. During the design phase, architects and developers can use the diagram to force out the system's object interactions, thus fleshing out overall system design. One of the primary uses of sequence diagrams is in the transition from requirements expressed as use cases to the next and more formal level of refinement. Use cases are often refined into one or more sequence diagrams. In addition to their use in designing new

systems, sequence diagrams can be used to document how objects in an existing (call it "legacy") system currently interact. This documentation is very useful when transitioning a system to another person or organization.

Diagram Elements:

- Object. Each of the objects that participate in the processing represented in the sequence diagram is drawn across the top. Note that objects are used in this diagram while classes are used in use cases, class diagrams, and state-transition diagrams.
- Lifeline. A dotted line is dropped from each object in the sequence diagram. Arrows terminating on the lifeline indicate messages (commands) sent to the object. Arrows originating on the lifeline indicate messages sent from this object to another object. Time flows from top to bottom on a sequence diagram.
- Active. To indicate that an object is executing, i.e., it has control of the CPU, the lifeline is drawn as a thin rectangle.
- Message. A horizontal arrow represents a message (command) sent from one object to another. Note that parameters can be passed as part of the message and can (optionally) be noted on the diagram.
- Return. When one object commands another, a value is often returned. This may be a value computed by the object as a result of the command or a return code indicating whether the object completed processing the command successfully. These returned values are generally not indicated on a sequence diagram; they are simply assumed. In some instances the object may not be able to return this information immediately. In this case, the return of this information is noted on the diagram later using a dotted arrow. This indicates the flow of information was based on a previous request.
- Conditional. Square brackets are used to indicate a conditional, i.e., a Boolean expression that evaluates to TRUE or FALSE. The message is sent only if the expression is TRUE.
- Iteration. Square brackets preceded by an asterisk (*) indicate iteration. The message is sent multiple times. The expression within the brackets describes the iteration rule.
- Deletion. An X is used to indicate the termination (deletion) of an object.

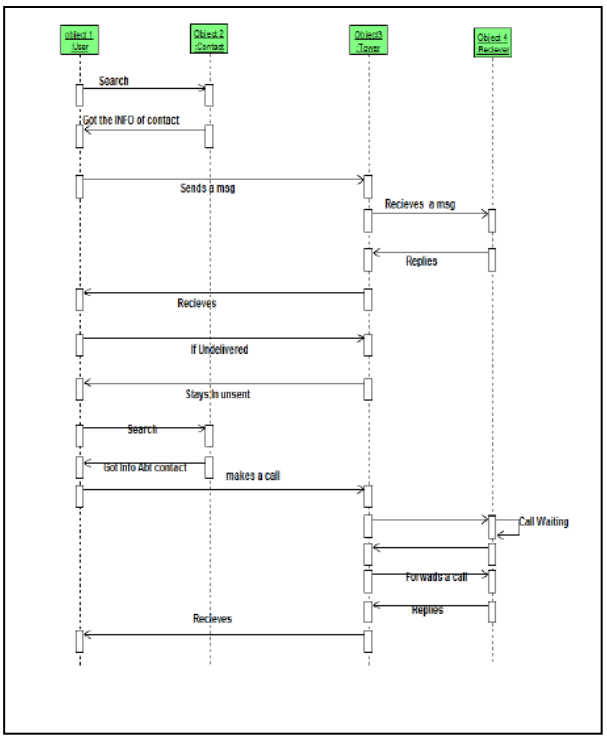


Fig 5 Sequence diagram for calling & messaging

The user in order to make a call or send a message, he needs to search the contact from the directory and get the info about the contact. Then, the message is sent to that particular contact, the message is sent to the tower before it reaches the contacts smart. Here the tower process includes in series of sequence but in the above sequence diagram it is shown in single object. But it is assumed as, if the other user is available within the same tower range. Then the message is passed to the other smarts inbox, where the message provides the necessary info about the sender's info. If the user wishes to reply to that message, he can do it as it done by the sender which repeats the same process. If the receiver's smart handset is not found then a failure notice is issued by the network providers to the users device where then the message is stored in outbox or unsent message (it is depended on the devices mechanism).

The user from the contact can also make call to another by searching the contact from the dictionary and fetching the information from the contacts. Then the call is passed from users smart to tower then to another device, if the other user attends the call. The user can proceed with the call or else the call can either be ended or made to wait until the previous call get over.

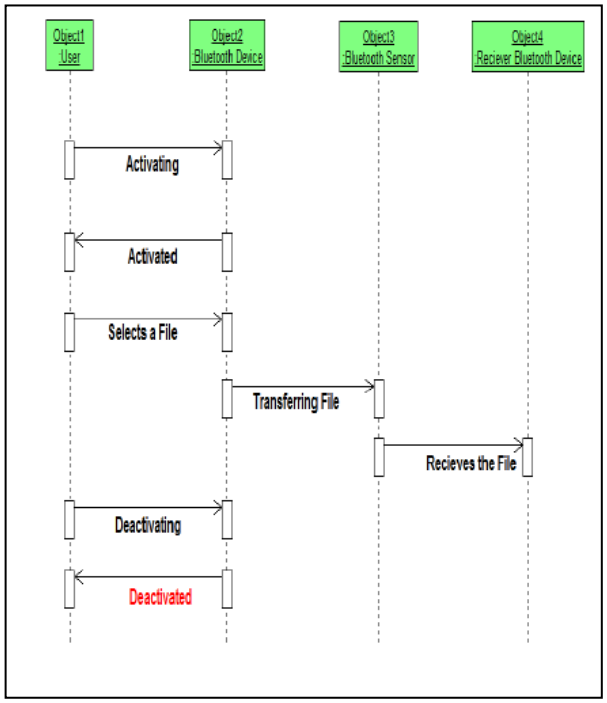


Fig 6. Sequence diagram for bluetooth communication

In order to establish the bluetooth communication, the user needs to activate the bluetooth device. So the activate command is passed to the device to initiate its process for communication. Then after the device gets active the control moves to the user so that the user can send a file which is then passed to the Bluetooth sensor from which the file is passed to another devices sensor and to the other users device. After sending the file, the Bluetooth device is deactivated.

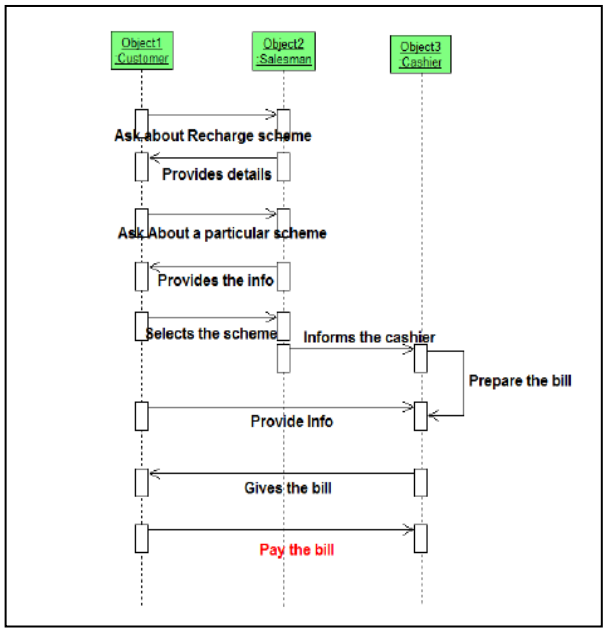


Fig 7. Sequence diagram for recharging

The above diagram shows how the recharge is done for smart to use the service for making the call or sending the message. The sequence flows as above, where the user asks the sales man for the schemes for recharge which suits the user needs.

The salesman then provides the details which the user can do the recharge by selecting any one from the list provided. Then, the recharge is made by providing the cash to get recharge coupon and does the recharge.

V. ACTIVITY DIAGRAM

UML 2 activity diagrams are typically used for business process modeling, for modeling the logic captured by a single use case or usage scenario, or for modeling the detailed logic of a business rule. Although UML activity diagrams could potentially model the internal logic of a complex operation it would be far better to simply rewrite the operation so that it is simple enough that you don't require an activity diagram. In many ways UML activity diagrams are the object-oriented equivalent of flow charts and data flow diagrams (DFDs) from structured development. Activity diagrams can show activities that are conditional or parallel. Activity diagrams should be used in conjunction with other modeling techniques such as interaction diagrams and state diagrams. The main reason to use activity diagrams is to model the workflow behind the system being designed. Activity Diagrams are also useful for: analyzing a use case by describing what actions need to take place and when they should occur; describing a complicated sequential algorithm; and modeling applications with parallel processes. However, activity diagrams should not take the place of interaction diagrams and state diagrams.

Activity diagrams do not give detail about how objects behave or how objects collaborate. Building block elements in an Activity Diagram are:

- Initial Node

An initial or start node is depicted by a large black spot.

- Final Node

There are two types of final node: activity and flow final nodes. The activity final node is depicted as a circle with a dot inside. The flow final node is depicted as a circle with a cross inside. The difference between the two node types is that the flow final node denotes the end of a single control flow; the activity final node denotes the end of all control flows within the activity.

- Fork and Join Nodes:

Forks and joins have the same notation: either a horizontal or vertical bar (the orientation is dependent

on whether the control flow is running left to right or top to bottom). They indicate the start and end of concurrent threads of control. A join is different from a merge in that the join synchronizes two inflows and produces a single outflow. The outflow from a join cannot execute until all inflows have been received. A merge passes any control flows straight through it. If two or more inflows are received by a merge symbol, the action pointed to by its outflow is executed two or more times.

- Decision and Merge Nodes:

Decision nodes and merge nodes have the same notation: a diamond shape. They can both be named. The control flows coming away from a decision node will have guard conditions which will allow control to flow if the guard condition is met.

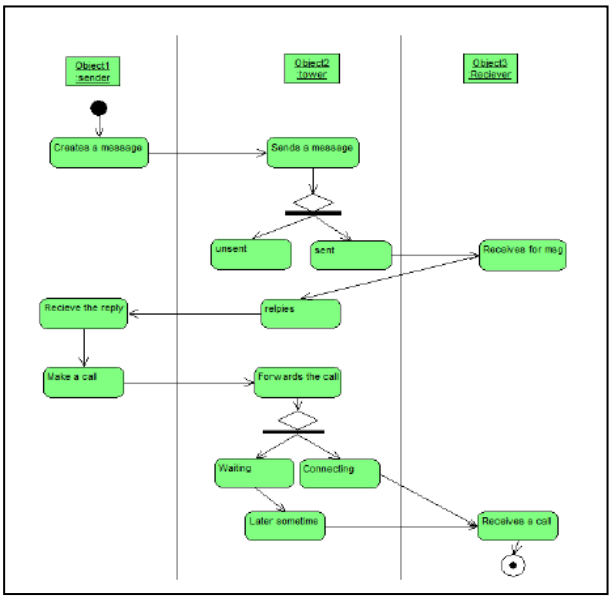


Fig.8 Activity Diagram for calling & waiting

The above is the activity diagram for contact where the user creates the message for sending it to the tower. The tower then searches for the other device, when the other device is found the message is delivered to the receiver. If not the tower waits for some time until the message gets expired where the expiry time is mentioned in the message itself by senders smart. If the message is not delivered, a failure notice is sent to the sender's smart. If the message is delivered, receiver can now see the message with senders contact information which is attached with the message. The user can then reply to the message as sender which repeats the same activity done by the sender.

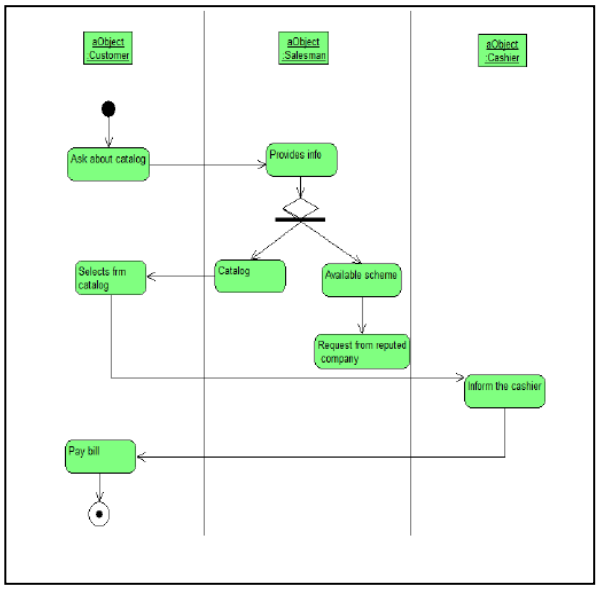


Fig. 9 Activity Diagram for a recharging

The above activity diagram shows, how the recharge activity is done by the user. The user asks for the catalog to the sales person, the sales person provides the recharge catalog to the user from which the user can select the scheme that suits the best to his/her requirement. The salesman can either get the scheme from the service provide through the portal given to him or from the pamphlet. The customer then selects the scheme and informs the salesman to recharge, in turn the sales person informs the cashier to collect the cash from the customer and provide the bill. So that the recharge is done for the customers smart.

VI. CONCLUSION AND FUTURE WORK

The paper has focused on the essential and extended Object Oriented features of a Smart phone Database Management System. Various models of UML have been employed to analyze the static, dynamic and functional view of the system.

In spite there are lot of functionalities rendered by mobile phones using recent emerging technologies,the mobilephones advancement deserves a major breakthrough.in a few years from now it is expected that mobile phones would replace most of the handheld systems,incorporating modern operating systems such as android 2.3 gingerbread,meego and windows phone and its emergent higher versions. Inorder to further enhance the features provided by the current day smartphones, an object oriented approach would add in the developmental growth .Our further work is focused on developing an ER modeling approach to implement with JAVA as a frontend and MY SQL , the online database as a backend and by establishing JDBC

connectivity.The same is planned to be tested using Rational Test Manager.

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❑❑❑

Developing Semantic Design of Best Railway Network System using Systematic Object Identification Strategy

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Abstract - For the betterment of the economic welfare, the database management act as a source to enrich the Indian railway reservation sectors. Implementing of this source to railway sector may establish the high economic status. Ensuring a high operational efficiency in the sector turns out to be the most essential goal for evaluating the organizational performance as a whole. This work aims to employ a modeling language aimed to provide a unified framework for representing a cheap and best railway management system, which implicitly ensures confidentiality of the information and messages. The proposed modeling methodology is based on the principle of database system, which allows for easy storage and retrieval of information. Furthermore, it is illustrated to provided an adequate formalization of its semantics, to describe structural and behavioral aspects of railway sector related to both logical and physical parts. It is needed to implement the software on the basis of Database system developed. Flaw in modeling process can substantially contribute to the development cost and time. The operational efficiency may be affected as well. Therefore special attention should be paid to the correctness of the models that are used at all planning levels and hence Unified Modeling Language (UML) takes its flawless role.

I. INTRODUCTION

Database management system is mainly used to overcome the data inconsistency and data redundancy in file documents. Database systems are designed to manage large bodies of information. Management of data involves both defining structures for storage information and providing mechanisms for the manipulation of information. It is also mainly used for highly secured data storage. The database language that is used by software developers, analysts, etc is the SQL language. The functional components of database management can be divided into the storage manager and the query processor components. Query processor is used to simplify the database to facilitate and access the data stored in it. Some of the elements in the storage manager are: authorization and integrity manager, transaction manager, file manager, buffer manager and its data structures used in it are: data files, data dictionary and indices.

The Unified Modeling Language is a standard visual modeling language intend to be used for

- Modeling business and similar processes
- Analysis, design and implementation of software based systems.

UML is mainly used to visualize the system design in multiple dimensions. So that the computer can understand the model before it is implemented into it. . The overall scope of the software can quickly and easily be defined at the start of the project with a high level model allowing for accurate estimation. It is appropriate for both new system developments and improvements to existing systems. This language was created by Rational Software in order to provide a standard in software engineering. It is now owned and controlled by the Object Modeling Group, an independent organization. UML has quickly become the de-facto standard modeling language in the software industry. UML is a universal language because it can be applied in many areas of software development. It includes user-definable extension mechanisms so that it can be adapted for specific environments. This language have three types of views for modeling a system in it. They are:

- Functional requirement view : It gives the functional requirements of the software from the client's point of view. This can be indicated by using use case diagram.
- Static structural view : It includes the static design of the software model i.e. it contains the objects, its

attributes and their functions. It can be represented using class diagrams and composite structure.

- Dynamic behavior view : It describes the system model with its dynamic behaviors. It can be represented using activity diagram and interaction diagram.

II. USE CASE DIAGRAM

Use case diagram describes the way a user interacts with the system by using a technique. A use case diagram simply describes particular functionality that the system is supposed to perform the dialog that a user or other entity will have with the system to be developed. Use case diagrams have four elements: actors, cases, extensions and uses.

- Actors : These are used to describe the role played by an external entity (eg: human users, hardwares like printers, etc). These can be specified using a 'stick man' symbol. For example: In a banking system, customer and the bank server are the actors.
- Case : The case contains the actions performed by the actors of the system. It specifies the functionality of the user within the system. This can be mentioned inside an elliptical shape. For instance, the online banking system has the customer(actor) who may deposit or withdraw the amount using their credit card number. Here the case is either deposition or withdrawal of money.
- Extensions : An extension extends a use case to illustrate a different perspective. It is optional for a use case diagram. For example: If a customer in an inventory, may pay the bill either with cash amount or by using credit card. Here, the options given to the customer is not necessary to mention and so we can simply have the case as the user pays the bill. This can be represented by <<extends>>.
- Use : This is actually a reuse of an already-defined use case.

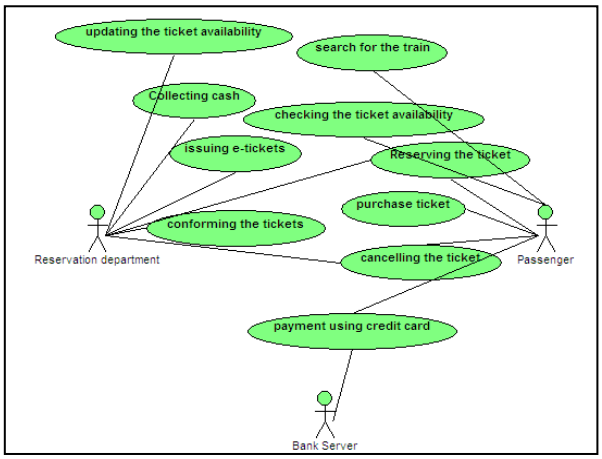

Fig. 1 : User case diagram for railway management.

The above use case diagram gives the overview of railway management system when people goes by the train, he would be requested to fill in registration form. He would have to provide details such as the passengers name, age, residential address, contact information, source, destination, train name, train no to the reservation department. The reservation department maintains a database for each reservation which contains information about the passenger details, the results of reservation undergone and the dates of travelling with the concerned train which would be available or not. The passengers would be directly get the ticket either conformation or waiting list. He performs to check the tickets available and also cancelling the tickets if the ticket would be conform orwaiting list and passengers identifies the ticket conformation. The payment of the ticket would be either by directly otherwise credit cards. The credit cards would be accepted by the bank server.

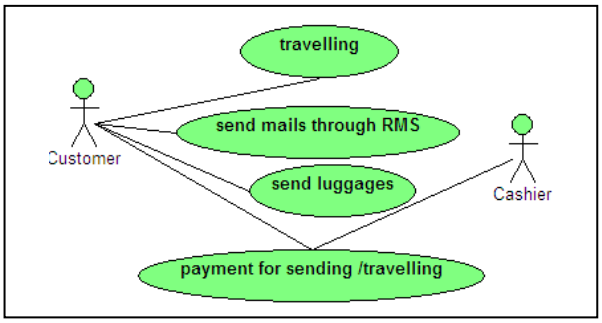

Fig. 2 : Use case diagram of the railway purpose

In railway management, management provides the facilities for both travelling and sending for people's purpose and for their convenient. In railway management, the customer send their parcel by RMS(Rail mail service),The management maintains the separate database for RMS service. In railway management, the management provides the goods train for sending luggages. The customer would be paid for sending travelling and RMS.

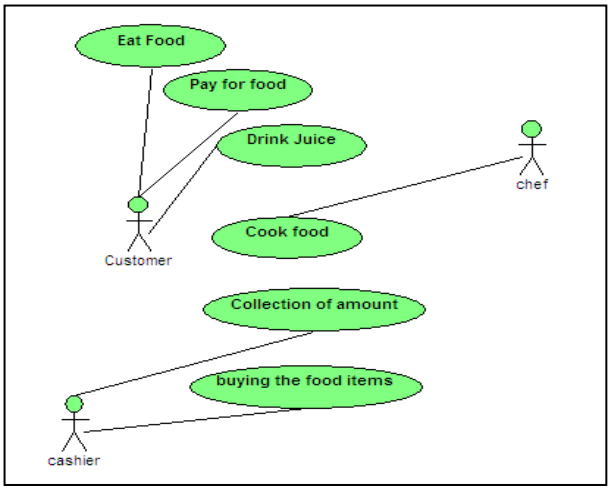

Fig. 3 : Use case diagram for railway canteen

The above use case diagram predicts the procedure in the railway canteen. Here the customer orders for the food. The chef takes the order and cooks food according to the order given by the customer. Then the chef provides the ordered food for the customer, then the customer eats the food and pays the amount to the cashier, then the cashier gives the bill.

III. INTERACTION DIAGRAM

Interaction diagram are used to illustrate interaction among classes. It describes the operations and behavior of the objects in the system design. It generates from each use case diagram to identify the messages and operations that represent the system's overall functionality.

SEQUENCE DIAGRAM : Sequence diagram shows the message flow from one object to another. It shows the sequence in which activities or behaviors occur. The elements used in the sequence diagram are:

- Lifeline : Lifeline is used to specify a object lifeline. It is depicted as a box at the top of a vertical line.
- Message : An arrow between two lifelines represents a message between two objects and it is labeled with messages name.
- Asterisk : Asterisk on the arrow indicates that the message is sent many times, to several different receiving objects.
- Self delegation : When the message arrow loops back to its starting box on the same object, the object is sending a message to itself; this type of message is called self delegation.

COLLABORATION DIAGRAM : In collaboration diagram the method call sequence is indicated by some numbering technique. The number indicates how the methods are called one after another. We have taken the same order management system to describe the collaboration diagram.

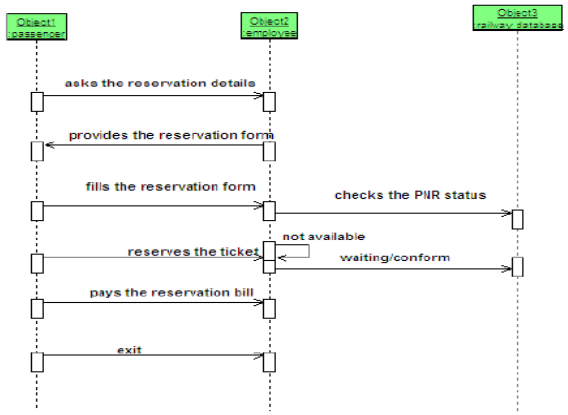

Fig. 5 : Sequence diagram for railway reservation.

The above sequence diagram deals about the procedure followed in railway reservation. The customer asks for the reservation details to the employee which in turn the employee provides the reservation form. The customer fills the reservation form according to the required details. The customer checks the PNR status. If the tickets are available, then the employee books the tickets for the customer. Finally, the customer pays the money.

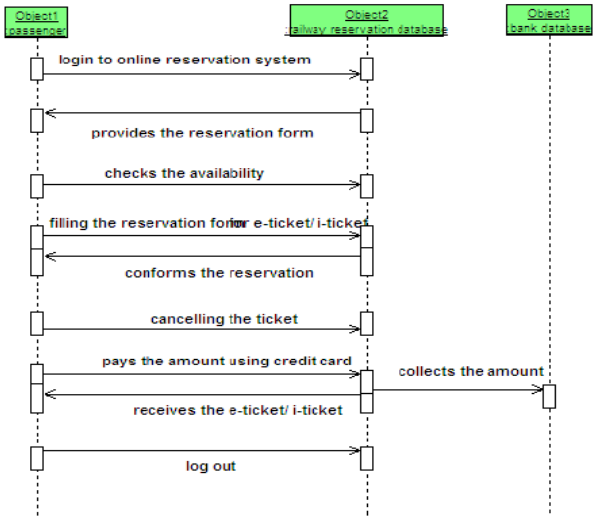

Fig. 6 : Sequence diagram for online railway reservation process.

The above diagram deals about the railway reservation for online booking. First the customer wants to log on to the online then an online reservation system provides a reservation form. The customer fills the details asked in the form. It checks the availability of seats with the online railway reservation database. If the seats are available, then it conforms the ticket. The amount for the tickets can be paid by credit cards. Then bank database system collects the amount for E/I ticket. The customer can also cancels the ticket, if the customer is not available. Finally the customer log outs from the railway online database.

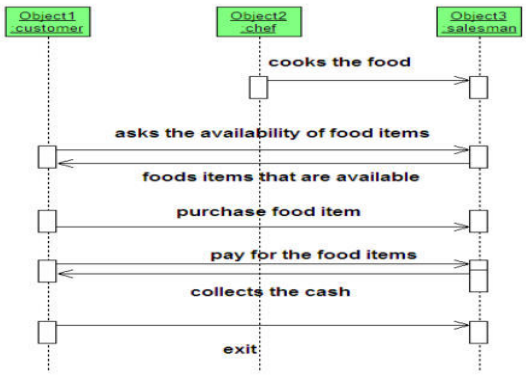

Fig. 7 : Sequence diagram for food process.

The above sequence diagram depicts the food process in railway system. The customer asks for the availability of food to the salesman . the salesman consults with the chef and informs the available food items to the customer. Then the customer the required food to the salesman and purchase the food item and pays the amount to the cashier.

IV. ACTIVITY DIAGRAM

UML diagram uses a activity diagram to model the flow of procedure or activity in a class. Activity diagram is another important diagram to describe dynamic aspects of the system in UML but not visualizing dynamic nature of a system. The activity diagram is suitable for modeling the activity flow of the system. An application can have multiple systems. Activity diagram are represent in the form of flow diagram which is flow from one activity to another activity. Activity diagrams deals with all type of flow control by using different elements like fork, join etc. The purpose of the activity diagram is to capture the dynamic behaviour of the system. It is similar to the sequences diagram and other three UML diagram. Activity diagram shows message flow from one activity to another but other diagram is used to show the message flow from one object to another. Activity diagram shows different flow like parallel, branched, concurrent and single. In activity diagram, the only missing is message part. When condition are used to decide which activity to invoke, the activity diagram uses to decide which node is to indicate the choice. It is used for the purpose to construct the executable system by using forward and reverse engineering techniques. This specific usage is not available in other diagrams. Activity diagrams do not give detail about how objects behave or how objects collaborate. Activity diagram is flow like a flow chart but activity diagram consists of some capabilities. Activity diagrams should be used in conjunction with other modeling techniques such as interaction diagrams and state diagrams. So the purposes can be described as:

- Draw the activity flow of a system.
- Describe the sequence from one activity to another.
- Describe the parallel, branched and concurrent flow of the system.

The parameters like activities, association, Conditions, Constraints are identified we need to make a mental layout of the entire flow. This mental layout is then transformed into an activity diagram. Following are the main usages of activity diagram:

- Modeling work flow by using activities.
- Modeling business requirements.
- High level understanding of the system's functionalities.

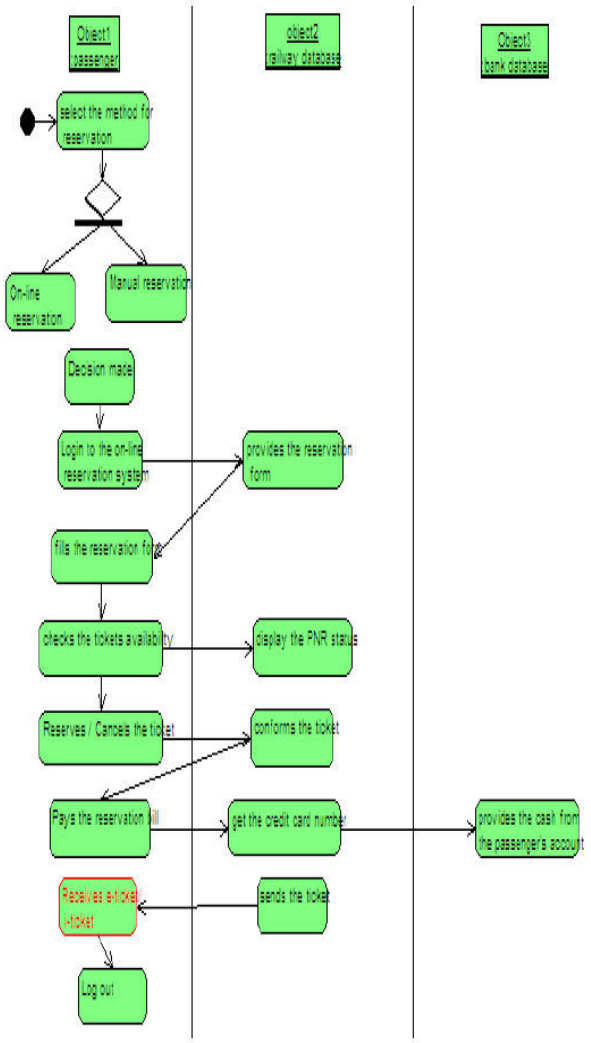

Fig. 8 : Activity Diagram for ticket reservation .

The above activity diagram deals about reserving a ticket. First the customer selects the method for reserving the ticket. A decision is made by the customer either to book via online or through manual. If the customer's choice is to book the tickets through online the customer should log in into online railway reservation database. The railway reservation database provides a form to the customer to fill the necessary details. the form is filled by the customer and submitted to the railway database for verification process. The railway reservation database checks for the availability and reports the status to the customer. If the customer books the ticket and pays the amount from his bank account through bank database and conforms the ticket.

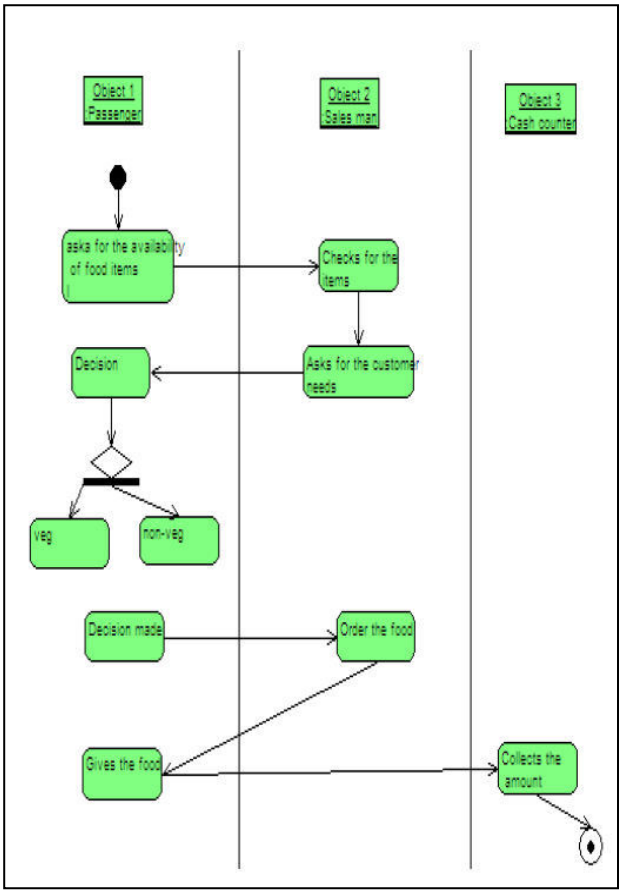

Fig. 9 : Activity Diagram for food process

The above activity diagram deals about food process. The passenger asks for the availability of food items to the salesman. Then the salesman checks the availability of food items and informs the passenger about the available food items. A decision is made by the passenger whether to choose veg or non-veg. then the passenger orders the food according to the wish of the passenger. The salesman provides the ordered food items to the passenger. the passenger pays the bill amount.

V. CONCLUSION AND FUTURE WORK

The paper has focused on the essential and extended database system features of a railway Management System. Various models of UML have been employed to analyze the static, dynamic and functional view of the system. In spite of several user-friendly, time-saving, cost-effective, convenient and flexible options provided by banks in the virtual space. Railway Management System has not achieved a major breakthrough that it deserves. However if the database approach is adopted while building the software, an explosive growth in railway Management System arena could be traced. Paper could be implemented using VB.net as front end and any reliable database system such as Oracle, as back end, and testing could be carried out by Rational Test Manager. The paper depicts the structural and behavioral aspects of online personal finance management system related to both logical and physical parts.. It is a fact that design flaws that surface during implementation are most costly to fix than those that are found earlier. Focusing on implementation issues too early restricts the design choices and often leads to inferior product. Hence the developed database approach encourages software developers to work and think in terms of application domain through most of the software engineering lifecycle. Since flaw in modeling process can substantially contribute to the development cost and time and affect the operational efficiency special attention is paid to the correctness of the UML models that are used at all planning levels rather than focusing much on implementation issues.

ACKNOWLEDGEMENT

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❑❑❑

Use of Controller Area Network Bus and Wireless Communication Technology to Improve Driving Safety

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Abstract - With more than one million people dying worldwide on the roads every year and lots of money in property loses, traffic safety remains an unsolved matter. The potentials of in-vehicle safety systems are currently investigated to improve this situation. Hence, embedded system which can collect some important context information and warn the driver in order to improve the safety of driving is needed. A Controller Area Network (CAN) bus with nodes of sensors or the node which is connected directly to the vehicle's CAN bus is very practical and reliable in terms of data Reliability . This context information should not be just kept in the vehicles; it should be shared with vehicles in the same neighbourhood or be sent to the information processing centre. In order to have a wireless communication, communication technologies like ZigBee, GPRS are needed to be used. In this paper, we propose a context aware system for improving road safety and efficiency as well as driving comfort.

I. INTRODUCTION

According to WHO statistics, every year more than 1.2 million people are killed in traffic accidents. According to a WHO forecast, traffic accidents will rank as the third biggest cause of deaths by 2020 [1]. Consequently, efforts are directed towards studying technologies that make possible the development of systems that help avoiding accidents or help the drivers to drive more comfortably.

In order to improve the safety of driving, "important" information needs to be presented to the driver, to the neighbourhoods' drivers or to the infrastructure. Therefore, in this paper, we propose a context aware system that is embedded on the vehicle and able to interact with the environment, collect information from the environment and it could also be able to send different of context information to the infrastructure V2I (or to the other vehicles V2V). This aims at enhancing safety by sending and receiving appropriate security information. This system consists mainly of an open Controller Area Network system and a wireless communication system and an embedded computer.

II. PROPOSED CONTEXT AWARE SYSTEM DESCRIPTION AND OPERATION

In our work, first a context aware system was proposed. A CAN bus was designed and realized with 3 nodes that allows the validation of the different electronic design and software solution. The CAN system constituted by 3 nodes could be used in this pervasive system. There is also a wireless communication system integrated in our system, ZigBee. Hence this system could be applied for collecting important information about the driving environment, the driver's information and information about the vehicle, and to send these informational messages to the driver or to other vehicles. Incorrect tire pressures can compromise the stability of a vehicle, it handling and braking, in extreme cases, could contribute to an accident. Briefly, if drivers are known or warned by such context information like , the pressure of vehicle's tires, status of the Brake many accidents will be avoided. The main idea of the proposed system is to exploit the driving context and collect some important context information.

Once context information achieves collecting, important and crucial information should not remain only inside vehicle; vehicles in the same neighbourhood should co-operate and share their information. Exchange context information between vehicles will confirm or reject current beliefs about the context or acquire new knowledge. So this co-operation increases the information of every vehicle, thus improving its decision making capabilities. Information can be passed onto the user as a warning or used for active intervention on the driving process. Hence, some communication technologies like ZigBee, GPRS are needed in our context aware system.

A. *Design of the embedded system in the vehicle*

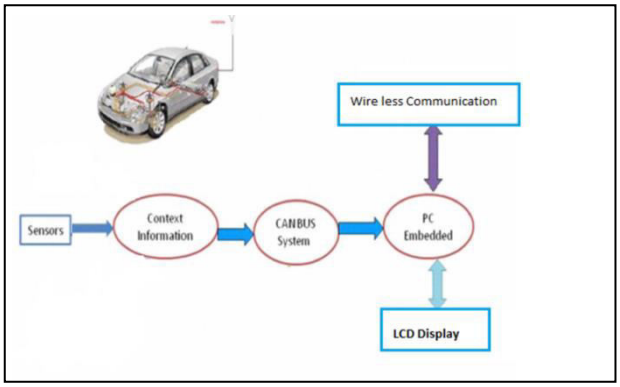


Fig. 1. System Architecture

Thanks to our today's technologies, there are quite a few of context information which can be collected. Kinds of sensors system offer a lot of important context information.

For example, a TPMS is a driver-assist system that warns the driver when the tire pressure is below or above the prescribed limits. A direct TPMS consists of sensors, radio frequency Transmitters and a receiver [II]. The pressure and the temperature of vehicle's tires can be gotten by the TPMS sensors system. Brake failure status can be obtained using fluid Level sensors (Leakage of Brake Fluid in the master cylinder). Accident Detection is done using Accelerometer Sensor. This information is send to the other vehicles.

For gathering all these context information messages in the embedded computer, a interface system is needed. According to CAN's characteristics, the CAN system is chosen. It's a vehicle bus standard designed to allow microcontrollers and devices to communicate with each other within a vehicle. So that it could have some nodes with sensors or actuators for realizing the information collection and the system control. The wireless communication system connects to the embedded computer in order to exchange information with external system. The wireless communication ZigBee is design for V2V communications,

A LCD display is used allowing this system to interact with the driver: Aware the driver (information from local sensors) Some other selected information (the position of vehicle, the vehicle speed, and the vehicle's stateA[1] or the road situation[2]) are transmitted to others vehicles by the communication modules.

[1] The vehicle is broken or in the case of accident

III. REALIZATION OF THE SYSTEM

A. *CAN Bus Overview*

CAN is a serial communication network system especially for connecting intelligent devices as well as sensors and actuators within a system or a sub-system. It is a high-speed network system consisting of two wires and a half duplex. It also meets the requirement of high speed applications in real time with short messages. Its robustness, reliability and the large following from the semiconductor industry are some of the benefits of CAN.The connection to the CAN bus is realized by using an encoder, CAN Transceiver (For example the MCP2551 in Microchip And TJA1040 in Philips), and a CAN controller. The controller can be integrated into a host-processor (microcontroller PIC 18F248, ARM7 LPC2129, etc.). In the Fig 3, Tx and Rx represent the message output and the message input in the CAN controller respectively.

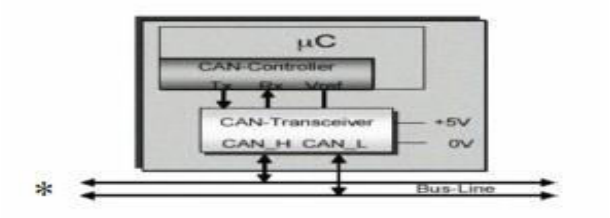
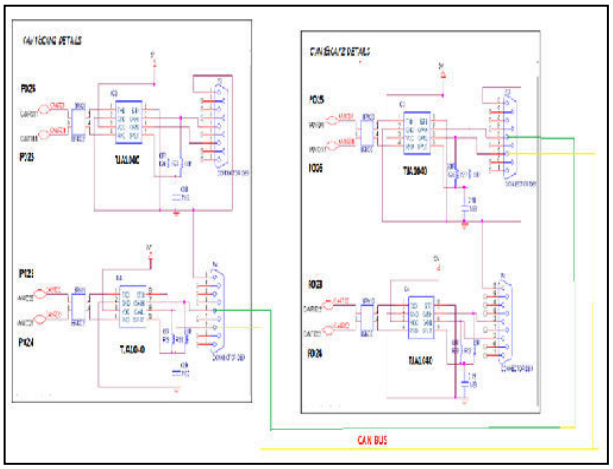


Fig. 2. CAN Node

B. *Realization of the CAN Bus*

The three Sensors were connected to the host processor: Tire pressure Sensor, Fluid level sensor, Accelerometer.



The Highest Priority assigned to Brake Status sensor. The Host Processor used was the LPC2129

[2] There is an accident on the road or an obstacle to pay attention

which has the inbuilt CAN controller. The CAN controller is connected to CAN Bus via the TJA1040 Transceiver. The information from the sensors was communicated via CAN Bus to the main Microcontroller which displays the information on the LCD Display.

C. Parameters to be measured

a. Brake status

b. Tire pressure

c. Accident information

a. Brake Status Monitoring

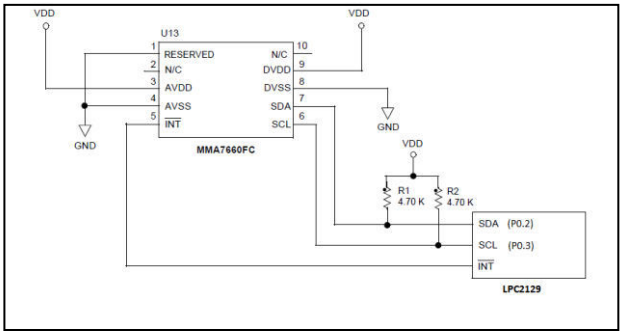
One of the parameter to indicate brake failure is the fluid level in the master cylinder, which should be 6 mm to 13 mm from the upper edge of the reservoir. Brake lining for the amount and pattern of wear is checked as the other parameters. There should be a minimum of 0.8 mm to 1.5 mm of lining at the thinner point above the rivets on riveted shoes. Type of fluid used in the reservoir are DOT3 (Department Of Transportation) (POLYGLYCOL FLUIDS) they absorb moisture, short storage life. DOT5 FLUID (SILICONE BASED FLUID) have high boiling point they do not absorb moisture, long storage life. Fluid level is measured using a fluid level sensor .The output of the voltage divider is given as the input to A/D converter. This measured value if below the prescribed level will be send via CAN bus to the main controller.

b. Tire Pressure Monitoring

Maintaining correct tire pressure for vehicle is very important factor i.e. will tell how much load it can safely carry .Correct tire pressure required for light 4 wheelers is 35 psi, up to 26 psi will indicate no warning. Incorrect tier pressure will eventually cause catastrophic tire failure, leading to: Hazardous incidents, Fuel consumption increases. Different ways to monitor tire pressure are Direct tire pressure monitoring, Indirect tire pressure monitoring. Sensors attached to each wheel .This method generates accurate warnings and alerts the driver instantly if pressure in any one tyre falls below the predetermined value due to puncture or rapid air loss. The pressure sensor placed inside the tire air chamber. This in turn acts as one CAN node. The pressure information send via CAN BUS to main controller where the information displayed on the LCD.

C . Accident Detection

The MMA7660FC is a ±1.5 g 3-Axis Accelerometer with Digital Output (I2C).This Accelerometer is interfaced to Host Processor through I^2C



Features

Low Power Current Consumption:

Off Mode: 0.4 µA,

Standby Mode: 2 µA,

Active Mode: 47 µA at 1 ODR

Low Voltage Operation:

Low Cost

D. Wireless Communication Module (Zigbee)

This Module is implemented using Xbee OEM Module from DigiKey. Zigbee is a Low cost , Low Power ,Mesh Networking Standard, based on IEEE 802.15.4 std. The modules require minimal power and provide reliable delivery of data between devices. The modules operate within the ISM 2.4 GHz frequency band and are pin-for-pin compatible with each other. The XBee OEM RF Modules interface to a host device through a logic-level asynchronous serial port.

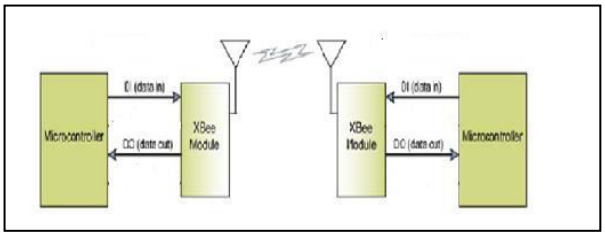


Fig.3 System data Flow in UART Interfaced

By default, XBee/XBee-PRO RF Modules operate in Transparent Mode. When operating in this mode, UART data received through the DI pin is queued up for RF transmission.

When RF data is received, the data is sent out the DO pin. If the module cannot immediately transmit (for instance, if it is already receiving RF data), the serial data is stored in the DI Buffer. Broadcast addressing is used and all the Xbee modules configured using X-ctu Software.

E .Processing Unit

In this section we discuss the microcontroller part.ARM 7 Microcontroller LPC2129has been used. There are three controllers in the system. Two are local controllers (LC1 and LC2) and third is main controller. The main purpose of local controllers is to collect data from sensors and transmit corresponding data to the main controller. Neither calculations are done nor warning generated in local controllers. All this happens in main controller. Output of signal conditioning units of alternator/battery status and temperature are used by LC1. LC2 is responsible for brake status and tyre pressure. The local controllers send data to main controller through CAN Bus at 1Mbps. Note that the local controllers are capable of handling more parameters and hence system can be expanded easily. The main controller's (MC) function is to receive data from local controllers, check for abnormal conditions, control the LCD display screen, produce warning messages on LCD.

IV. SIMULATION RESULTS

The Status of A/D CONVERTER , CAN NODE1 AND CAN NODE 2 is as shown below in Fig.6.1, Fig.6.2

The status of various Control Registers, Status Registers of A/D Conveter0 is observed. At the same time Analog value converted to Digital value at CAN Node 2 is transmitted and received by CAN Node 1

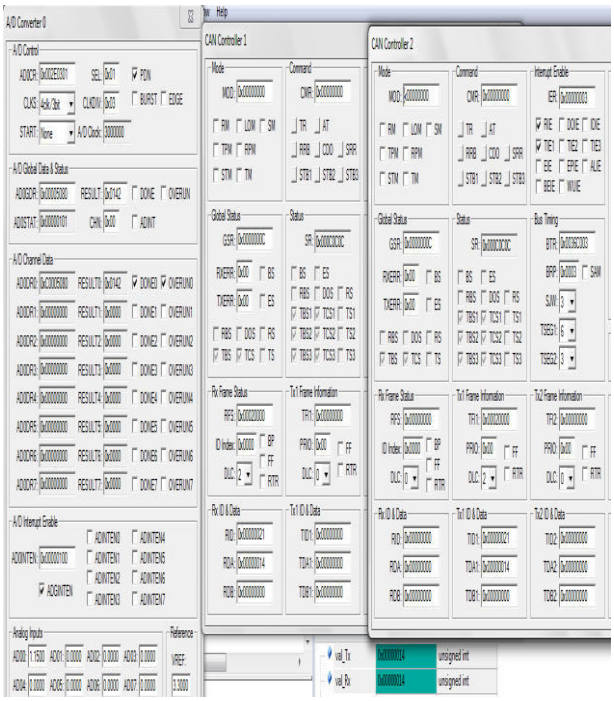
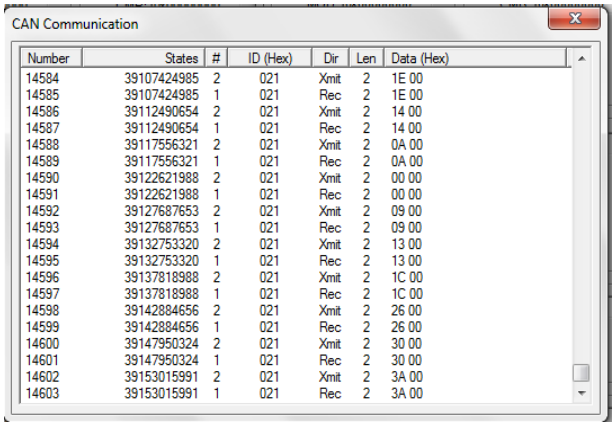


Fig.4. Output for Analog Voltage value=1.15V

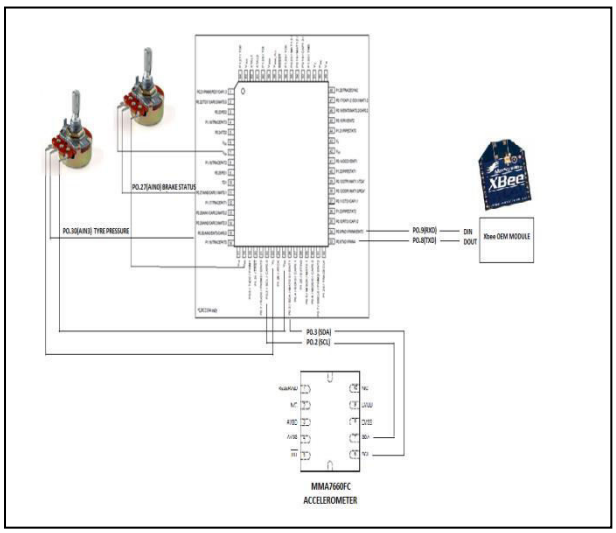


Number	States	#	ID (Hex)	Dir	Len	Data (Hex)
14584	39107424985	2	021	Xmit	2	1E 00
14585	39107424985	1	021	Rec	2	1E 00
14586	39112490654	2	021	Xmit	2	14 00
14587	39112490654	1	021	Rec	2	14 00
14588	39117556321	2	021	Xmit	2	0A 00
14589	39117556321	1	021	Rec	2	0A 00
14590	39122621988	2	021	Xmit	2	00 00
14591	39122621988	1	021	Rec	2	00 00
14592	39127687653	2	021	Xmit	2	09 00
14593	39127687653	1	021	Rec	2	09 00
14594	39132753320	2	021	Xmit	2	13 00
14595	39132753320	1	021	Rec	2	13 00
14596	39137818988	2	021	Xmit	2	1C 00
14597	39137818988	1	021	Rec	2	1C 00
14598	39142884656	2	021	Xmit	2	26 00
14599	39142884656	1	021	Rec	2	26 00
14600	39147950324	2	021	Xmit	2	30 00
14601	39147950324	1	021	Rec	2	30 00
14602	39153015991	2	021	Xmit	2	3A 00
14603	39153015991	1	021	Rec	2	3A 00

Fig. 5. CAN Communication Window

V. HARDWARE IMPLEMENTATION

- LPC2129 arm development board from NSK electronics.
- Two 10 k Potentiometer(Brake and Tyre Pressure)
- Two multistranded wires.
- Accelerometer(MMA7660FC) from freescale
- Xbee OEM RF modules



The two development boards were interfaced through CAN bus. Can node2 is the transmission node Can node1 is the receiving node.10 K potentiometer was connected to channel 0 (AIN0) and channel 3 (AIN3)of LPC2129. POT connected to channel 0 is used to indicate the Brake status. POT connected to channel 3 is used to indicate the Tyre Pressure status .Highest priority is given to the POT connected to channel 1.

Varying the potentiometer, the A/D CONVERTER output was transmitted from CAN NODE2 via CAN BUS and received by the CAN NODE 1.Transmitted data and Received data was observed on the LCD. For value of below 256 , ABNORMAL is displayed on the LCD. For the value of above 256, NORMAL is displayed ON THE LCD. Accident Detection is done using the Accelerometer Module for the following conditions Left ,Right, Front and Shake. This information is transmitted wirelessly using the Xbee OEM Module and received by the receiver end, accident displayed on the LCD.

VI. CONCLUSION

A pervasive CAN system is proposed for collecting the important information, warning the driver and sending these informational messages to the other vehicle or an information centre. This context aware system is composed of a CAN bus system, a wireless communication system. 3 nodes of CAN bus have already been realized with some tests.. An experimental test has been made to verify the operation of the proposed system. By a ZigBee communication technology, two vehicles communicated and warned drivers with their context information which comes from our realized pervasive CAN system. Hence, this system could be embedded into the vehicle following our prototype in order to increase the safety on the road.

The above proposed system could also be implemented using RTOS and ARM9 Development Kit mini2440 from Friendly Arm. Additional causes of accidents could be taken care of like: Task-Detection of Vehicle approaching from the opposite direction on a Blind Curve, Task 2-To avoid attending a phone call while Driving .If the above two tasks are activated at the same time Priority is given to first task. The system would be efficient if large no of tasks are multitasked.

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Voltage Stability Improvement using Design and Implementation of 1 kvar Synchronous Phase Modifier (SPM) and finding its Optimal Location in Power Systems using Voltage Collapse Proximity Index (VCPI)

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Abstract **-** Reactive power control is the basic requirement for maintaining the voltage levels thereby the stability of the interconnected power system. Voltage variations can be stabilized and controlled by providing required reactive power. These low voltages may also reduce the power Transfer through the transmission lines and may lead to Instability. Voltage stability has recently become a challenging problem for many power systems. Voltage instability is one phenomenon that could happen in power system due to its stressed condition. The result would be the occurrence of voltage collapse which leads to total blackout to the whole system.

Single Machine Single Bus (SMSB) Test System is setup in the laboratory to evaluate the Synchronous Phase Modifier (SPM) on improvement of bus voltage and its stability. It comprises of a 3-phase Synchronous Machine of 5kva capacity and a 3-phase squirrel cage Induction Motor of 5HP Rating. Brake test have been performed on the Induction Motor by taking the supply from the Synchronous Generator. The bus voltage is fall down from 425V to 390V on Full Load. SPM have been designed and tested by connecting it to SMSB Test System and experimental results have been presented in this paper. The Power – Voltage (P-V) curves of the SMSB Test system with and with out SPM is tested and results have been presented in the paper which shows the effectiveness of SPM.

The second part of this paper is focused on the Contingency ranking which is one of the important issue of voltage stability. Contingency table have been drawn for (n-1) contingencies and ranked them based on VCP Iindex and identified the severe most contingency. Voltage stability of the system has been enhanced by providing reactive power compensation using Synchronous Phase Modifier (SPM) at the optimal location. The voltage stability has been improved for severe most contingency.

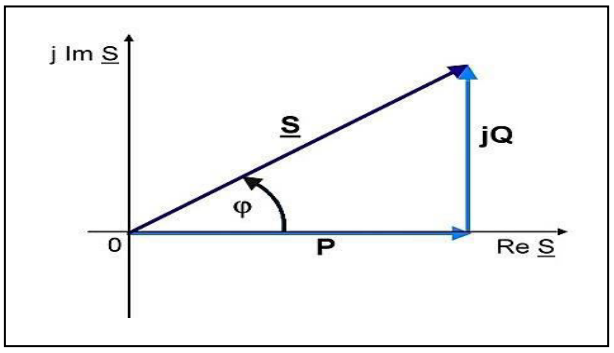
Keywords: *Voltage Stability Enhancement, Contingency Analysis, Contingency Ranking, Voltage Stability Improvement for most severe contingency, Reactive power control, SPM, Optimal placement of compensation device.*

I. INTRODUCTION

Reactive power (vars) is required to maintain the voltage to deliver active power through transmission lines. When there is not enough reactive power, the voltage sags down and it is not possible to push the power demanded by loads through the lines. Many devices contribute to systems reactive power and voltage profile.

I.1. Reactive power

The Reactive Power plays a vital role in maintaining voltage stability. The figure.1 represents the Power Triangle. Reactive power does not transfer energy, so it is represented as the imaginary axis of the vector diagram. Real power moves energy, so it is the real axis.



I.2. Significance of Reactive Power

Many devices contribute to reactive power compensation and voltage profile. A transmission line, due to its physical characteristics, supplies reactive power under light loading and consumes it under heavy loading conditions. Power system voltages are

controlled through the supply and consumption of reactive power. In general terms, decreasing reactive power margin causes voltage fall, while increasing reactive power margin causes voltage rise. A voltage collapse occurs when the system is trying to serve much more load than the voltage can support.

To maintain efficient transmission and distribution, it is necessary to improve the reactive power balance in a system by controlling the production, absorption, and flow of reactive power at all levels in the system.

II. VOLTAGE INSTABILITY

Voltage stability is concerned with the ability of a power system to maintain acceptable voltage at all buses in the system under normal conditions and after being subjected to disturbance.Voltage instability is basically caused by an unavailability of reactive power support in an area of the network, where the voltage drops uncontrollable. Lack of reactive power may essentially have two origins: firstly, a gradual increase of power demands without the reactive part being met in some buses or secondly, a sudden change in the network topology redirecting the power flows in such a way that the required reactive power cannot be delivered to some buses.

Instability that may result occurs in the form of a progressive fall or rise of voltages of some buses. A possible outcome of voltage instability is loss of load in an area, or tripping of transmission lines and other elements by their protective systems leading to cascading outages. Loss of synchronism of some generators may result from these outages or from operating conditions that violate field current limit. A situation causing voltage instability occurs when load dynamics attempt to restore power consumption beyond the capability of the transmission network and the connected generation.

Many power system blackouts all over the world have been reported where the reason for the blackout has been voltage instability.

1) WSCC USA July 2 1996: A short-circuits on a 345 kV line started a chain of events leading to a break-up of the western North American power system. The final reason for the break-up was rapid overload/voltage collapse/angular instability.
2) Florida USA 1985: A brush fire caused the tripping of three 500 kV lines and resulted in voltage collapse in a few seconds

The driving force for voltage instability is usually the loads. In response to a disturbance, power consumed by the loads should be restored. Voltage stability problems normally occur in heavily stressed systems. While the disturbance leading to voltage collapse may be initiated by a variety of causes, the underlying problem is an inherent weakness in the power system. One of the most important problems is Contingency and it's ranking. It has been done using VCPI for IEEE–9 bus Test system.

II.1. Stability Indices

II.1 .a) P-V curve

As the power transfer increases, the voltage at the receiving end decreases. Finally, the critical or nose point is reached. It is the point at which the system reactive power is out of use. The curve between the variations of bus voltages with output power (P) is P-V curve or 'Nose' curve. PV curves are used to determine the loading margin of the power system. The margin between the voltage collapse point and the current operating point is used as voltage stability criterion.

II.1.b) Voltage Collapse Proximity Index VCPI

The VCPI investigates the stability of each line of the system and they are based on the concept of maximum power transferred through a line.

$$VCPI = P_r/P_{rmax} \qquad (1)$$

Where the values of P_r and Q_r are obtained from conventional power flows calculations, and $P_{r(max)}$ and $Q_{r(max)}$ are the maximum active and reactive power that can be transfered through a line. The VCPI indices varies from 0 (no load condition) to 1 (voltage collapse).

III. SYNCHRONOUS PHASE MODIFIER

Synchronous condenser is a synchronous motor that is not attached to any other driven equipment. Its field is controlled by a voltage regulator to either generate or absorb reactive power as needed to support a system's voltage or to maintain the system power factor at a specified level. The condensers installation and operation are identical to large electric motors.

Increasing the device's field excitation results in its furnishing magnetizing power to the system. Their principal advantage the ease with which the amount of correction can be adjusted. The energy stored in the rotor of the machine can also help to stabilize a power system during short circuits or rapidly fluctuating loads such as electric arc furnaces.

As the load on a synchronous motor increases, the armature current I_a increases regardless of excitation. For under and over excited motors, the power factor tends to approach unity with increase in load. The

change in power factor is greater than the increase in I_a with increase in load. The magnitude of armature current varies with excitation. The current has large value both for high and low values of excitation. In between, it has minimum value corresponding to a certain excitation. The variations of I with excitation are known as V curves because of their shape. For the same output load, the armature current varies over a wide range and so causes the power factor also to vary accordingly. When over-excited, the motor runs with leading power factor and with lagging power factor when under-excited. In between the power factor is unity. The minimum armature current corresponds to unity power factor.

An over-excited motor can be run with leading power factor. This property renders it extremely useful for phase advancing purposes in the case of industrial loads driven by induction motors and lighting and heating rods supplied through transformers.

III.1. Operation of Synchronous Phase Modifier

A variation in the excitation of a synchronous motor alters the power factor at which motor operates. As the excitation of the machine is increased, the power factor passes from a lagging, through unity, to a leading power factor. This characteristic of the synchronous motor is used to correct the power factor of the loads taking lagging current. When used in this way the synchronous motor is usually run without any mechanical load and its excitation is adjusted so that it operates at a leading power factor. Such a motor is termed as synchronous phase modifier. When the synchronous motor is used as a means of controlling the voltage of a transmission line the term synchronous phase modifier or synchronous compensator.

IV. DESIGN OF SPM

The design of SVC is based on our test system Requirements. For any system find the variation of reactive power with load variations i.e $Q_d = (Q_1,Q_2,.., Q_n)$.Whare Q_d is the Reactive Power Demand and Q_1, Q_2, ..., Q_n are the variations in demand.

Set the Reference Voltage it may be set to 1.0 p.u or as closer as possible to it and find corresponding Reactive Power demand. Set reference reactive power Q_{ref} as 1.0 p.u (corresponding to voltage value of 1.0 p.u).

The fixed Capacitor (FC) value of the SVC can be obtained as $Q_{spm} = Q_{max} - Q_{ref,}$ Where Q_c is the Reactive Power supplied by the SPM.

V. CONTINGENCY ANALYSIS

Disturbances that might happen on a power system:

- Loss of a line
- Loss of a transformer
- Loss of a generating station
- Loss of a major load

Line outage in power system lead to the voltage collapse which implies the contingency in the system. Line outage contingencies are ranked so that the line which highly affects the system when there is an outage occurs in this line in terms of voltage instability could be identified. The contingency ranking process can be conducted by computing the line stability index of each line for a particular line outage and sort them in descending order. The contingency which is ranked the highest implies that it contributed to system instability.

One of the most important factors in the operation of a power system is the desire to maintain system security. System security involves practices designed to keep the system operating when components fail. Also, if a transmission line is damaged and taken out by relaying, the remaining transmission lines can take the increased loading. Many possible outage conditions could happen to a power system. Thus, there is a need to have a mean to study a large number of them, so that operation personnel can be warned ahead of time if one or more outages will cause serious overload on other equipments. The problem of studying all possible outages becomes very difficult to solve since it is required to present the results quickly so that corrective actions could be taken. Contingency analysis procedures model single failure events, one after the other in sequence until all credible outages have been studied. The most difficult problem is the selection of these credible outages.

"The worst single contingency is the one that causes the largest decrease in the reactive power margin". Contingency screening and ranking is one of the most important components of VSA. The purpose of contingency screening and ranking is to determine: which contingencies may cause power system limit violations and/or system instability according to voltage stability criteria. The margin between the voltage collapse point and the current operating point is used as the voltage stability criterion.

Contingencies are ranked according to their margins to voltage collapse. A margin to voltage collapse is defined as the largest load change that the power system may sustain at a bus or collection of buses from a well defined operating point. The operating point may be

obtained from a real-time operating condition or from a postulated condition computed from a system simulation. The margin may be measured in MVA, MW, or MVAR.

This paper simulates IEEE 9 Bus Test System using mipower software. The severe most contingency is identified based on Voltage Collapse Proximity Index (VCPI). The optimal placement of compensation device is obtained based on VCPI values. The maximum of VCPI index value gives the best location for compensation. By placing a shunt capacitor at 8th bus the voltage stability has been improved tremendously.

VI. CASE STUDY: TEST RESULTS

VI.1 SMSB Test System Experimental Results

The SMSB test system is initially tested without any SPM and obtained the results also P-V Curves have been drawn. Secondly the same system is tested by connecting an SPM and P-V curves have been drawn.Fig.2 shows the SMSB Test system and Fig.3 shows the same test system with SPM. Table.1 and Table.2 shows the corresponding test results.

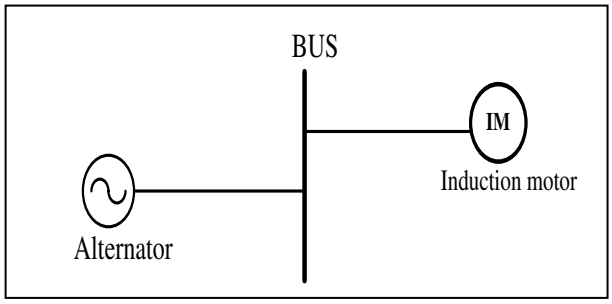


Fig.2 SMSB Test System without SPM

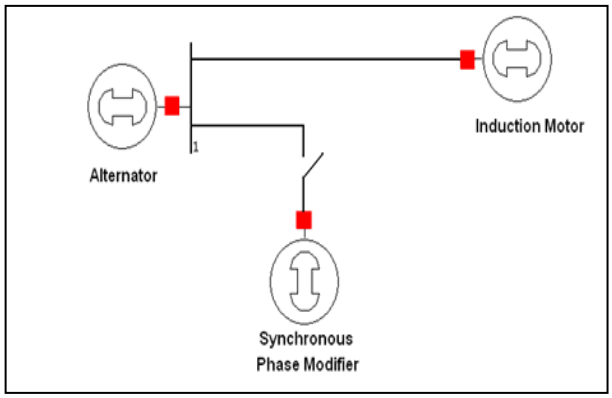


Fig.3 SMSB Test System with SPM

Table-1: SMSB Test system results without SPM

S.No	V (V)	V(p.u)	Active power(W)	Load Current (A)
1	415	1.0	240	3.5
2	400	0.96	560	4.5
3	390	0.94	1000	5.5
4	375	0.90	1500	6.5

Table-2: SMSB Test system results without SPM

S.No	V (V)	V(p.u)	Active power(W)	Load Current (A)
1	415	1.0	200	3.0
2	415	1.0	500	4.0
3	412	0.99	980	5.0
4	412	0.99	1400	6.0

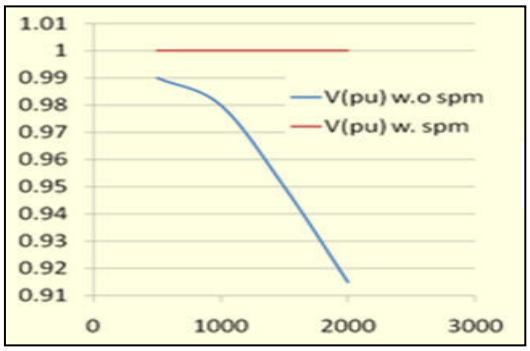


Fig.4 P-V Curves with and without SPM

VI.2 IEEE 9 Bus Test System Results

Fig.5 shows the IEEE 9-Bus Test System with one slack bus and two generator buses and three load buses.

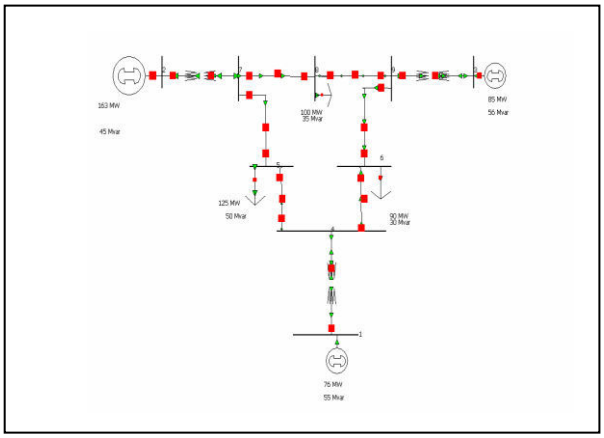


Fig.5 IEEE 9 Bus Test system

The contingency ranking

Table.3:N-1Contingency-Ranking

Line Outage	VCPI Values								
	7-5	2-7	3-9	7-8	4-1	6-4	8-9	9-6	5-4
Bus 4	0.404	0.098	0.164	0.064	0.167	0.044	0.062	0.119	0.072
Bus 7	0.363	0.295	0.093	0.092	0.075	0.011	0.050	0.040	0.029
Bus 5	0.636	0.278	0.153	0.101	0.139	0.041	0.101	0.108	0.088
Bus 6	0.329	0.189	0.261	0.178	0.196	0.260	0.094	0.206	0.118
Bus 9	0.240	0.217	0.248	0.216	0.192	0.233	0.087	0.031	0.103
Bus 8	0.249	0.345	0.259	0.360	0.220	0.222	0.219	0.103	0.149

Table.3 Simulation results by placing SPM at two ill buses (at 5th and 8th Bus)

Bus no.	PU Voltage	Bus Voltage (KV)	Total Losses
1	1.00	138.0	Active Power Loss is 35.6MW
2	1.00	138.0	
3	1.00	138.0	Reactive Power Loss is 91.0 Mvar
4	0.93	128.5	
5	0.86	118.6	
6	0.90	125.1	
7	1.00	138.1	
8	0.88	122.4	
9	0.95	132.0	

V. CONCLUSION

IEEE 9 Bus Test System is simulated in MI-POWER Software with base case and (n-1) contingencies.

Contingency table have been drawn for (n-1) contingencies and ranked them based on VCPI at all buses. Identified the severe most contingency based on voltage stability analysis.

Voltage stability of the system has been enhanced by providing reactive power compensation at two ill buses i.e. 5th and 8th buses. The voltage stability of the power system has been improved.

VI. FUTURE SCOPE

The Design and implementation of SPM can be extended for the large systems. The critical most contingency can be identified based on other voltage stability induces.

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An Effective Bufferless Routing using Unicast Based Multicast Method

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Abstract - Network on Chip [NoC] is a new technology that embeds heterogeneous interconnected cores. It advantage over System on Chip [SoC] are that Network on Chip provides modularity, higher performance, better structure and compatibility with core design and reuse. Previous on chip interconnection network commonly assumed that each router in the network needs to contain buffers, where packets are transmitted from buffer to buffer within the network. This increases the complexity of the network design. To overcome this complexity, bufferless routing is used in unicast based multicast routing algorithm. This work discusses the impact of power reduction.

Keywords-*Network on Chip, System on Chip, Buffer Routing, Bufferless routing,Unicast Based Multicast.*

I. INTRODUCTION

VLSI stands for Very Large Scale Integration. This field involves more and more logic devices into smaller and smaller area. VLSI categorized System on Chip, can integrate hundreds of cores into single chip this communicate by buses. A bus cannot have more than one access at the same time, which means that concurrent transactions are not allowed, one transaction will have access to the bus at a certain moment. A new paradigm is introduced, Network on Chip to solve the SoC problems. Network on Chip (NoC) is becoming a solution to nowadays bus-based communication infrastructure limitations. NoC architecture is possible to develop the hardware of resources independently as standalone blocks and create the NoC by connecting the block as element in the network. Moreover, the scalable and configurable network is a flexible platform that can be adapted to the needs of different workloads, while maintaining the generality of application development method and practices.

A two dimensional mesh interconnection topology is simplest from a layout perspective and the local interconnection between resources and switches are independent of the size network. Moreover, routing in a two-dimensional mesh is easy resulting in potentially small switches, high bandwidth, short cycle and overall scalability. A NoC consists of resources and switches that are directly connected such that resources are able to communicate with each other by sending messages. A resource is a computation or storage unit. Switches route buffer messages between resources. Each switch is connected to four neighboring switches through input and output channels. A channel consists of two one dimensional channel point to point buses between two switches or a resource and a switch. Switches may have internal queues to handle congestion. We expect the size of a resource to shrink with every new technology generation. Consequently the number of resources will grow, the switch-to-switch and the switch-to-resource bandwidth will grow, but the network wide communication protocols will be unaffected.

Arbitrary computation elements can be connected to the communication network. NoC based system may contain processor cores, DSP cores, memory banks, specialized input/output blocks such as Ethernet or Bluetooth protocol stack implementation, graphic processor, FPGA blocks etc. The size of the resource can range from a bare processor core to local cluster of several processors and memory connected via local bus.

The reuse of processor cores has been developed by defining bus interfaces. By defining network interfaces, NoC takes this concept further because it allows integrating an arbitrary number of resources into network. In bus based system adding a new has a profound impact on the performance of the rest of the system because the same communication resources are shared among more resources. In a NoC adding a new

resource also means to add new communication capacity by adding new switches and interconnect.

A NoC provides support for message-passing in such cores, and also allows for spatial reuse, whereby communication among various modules can occur concurrently over a distributed collection of wires. There are several routing algorithm for communication to deliver the data. In routing algorithm unicast method is used to deliver the packet from single source to single destination, multicast method is used to deliver the single source to group of destination and broadcast method is used to deliver the single source to the entire destination.

The main contributions of the paper include: The test data delivery and the test responses are delivered along the reverse paths in the unicast based multicast tree back to the ATE,where test responses are compacted further on the way to the ATE without any extra hardware in the NoC is proposed.

II. RELATED WORK

Many of the literature on NoC have discussed about various multicast techniques, buffered and bufferless routing techniques. A summary of these methods are discussed below

In recent years, A number of routing algorithm are discussed for data delivery. Amirali Habibi and Mohammad Arjomand [1] proposed multicast scheme. In a multicast scheme, a set of unique multicast tuples is in the form of m=<s, D> where s refers to an IP core sending a message to all cores in set. This approach includes two phases. In the first phase, the outgoing bandwidth of each source node is modified with respect to its multicast operations. Then, a heuristic algorithm to effectively map IP cores on NoC nodes based on the estimated outgoing bandwidth takes place.

Wenmin Hu and Zhonghai [2] proposed in tree based multicast. In a tree based multicast scheme is a tree structure built representing shortest path among nodes, and a loop-free distribution structure. There are two power efficient tree based multicast routing algorithms, Optimized tree (OPT) and Left XY-Right-Optimized tree (LXYROPT) are also proposed. XY tree-based (XYT) algorithm and multiple unicast copies (MUC) are also implemented on the router as base. Tree based multicast requests extra virtual channels. Tree based is inefficient.

Tzung-Shi Chen and Chih-yung chang [3] proposed in path based multicast scheme. In a path based multicast tree there are two proximity grouping they are graph based proximity grouping and pattern based grouping. Graph-based proximity is used to group the destination with locality together to construct several disjoint sub meshes. They are source to leader and leader to destination. Pattern-based grouping proposed to exploit the spatial locality of the destination set. Pattern based grouping is next presented to explore the destination set in order to form groups with proximity relations based on the pattern classification scheme. The path based multicast scheme is inefficient.

Po-Tsang Huang and Wei Hwang [4] proposed buffered routing. In buffered routing buffers are used to store and forward according to frequency of the receiver and the transmitter. Traditionally, In NoC Transmitter core and Receiver core must be synchronized, for this purpose buffers are used. Buffers store and forward the data according to the frequency of the receiver. In buffer communication there are different switching techniques. The buffer process leads to limitations in the existing system like increased memory size, increased power consumption and complexity in network design.

Thomas Moscibroda and Onur Mutlu [5] proposed bufferless routing. In bufferless routing there are two techniques. They are flit-bufferless technique and wormhole bufferless technique. In flit-bufferless technique large packets are broken into small pieces called flits. The first flit, called the header flit holds information about this packet's route and sets up the routing behavior for all subsequent flits associated with the packet. The head flit is followed by zero or more body flits associated with the packet. The head flit is followed by zero or more body flits, containing the actual pay load of data. The final flit, called the tail flit, performs some book keeping closing the connection between the nodes. And in Wormhole-bufferless technique, it does not dictate the route to the destination but decides when the packet moves forward from the router. Advantage of this bufferless routing an entire packet need not to be buffered to move on to the next node, increasing throughput and channel allocation are decoupled.

III. PROBLEM FORMULATION

The main problem addressed in this paper is formulated as follows: Most of the work on chip uses buffer for communication. A buffer stores the data and forwards the packet to the next node. Buffers on chip consume significant energy, occupies chip area and increases design complexity. The problem is to device a bufferless routing in order to reduce the complexity by using a bufferless unicast based multicast method.

IV. PROPOSED METHOD

To reduce the power in NoC based on bufferless routing in unicast based multicast scheme. In bufferless routing the buffer are eliminated and information regarding the frequency allocation is informed to the

receiver core by the transmitter core by using the unicast based multicast scheme. A unicast based multicast scheme completes multicast by using multiple unicast. It delivers a packet from a single transmitter core to several receiver cores. Figure 1 and Figure 2 shows model of buffered and bufferless routing where T_1, T2, T3 …Tn and R_1, R2, R3…….Rn represent transmitting cores and receiving core respectively.

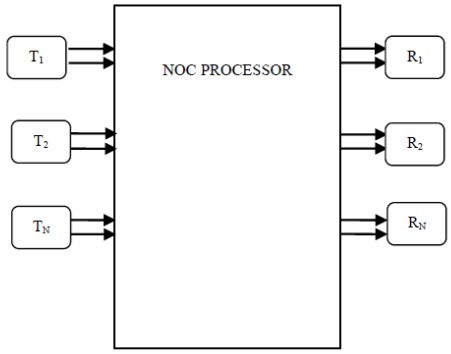

Figure 1Bufferless Routing

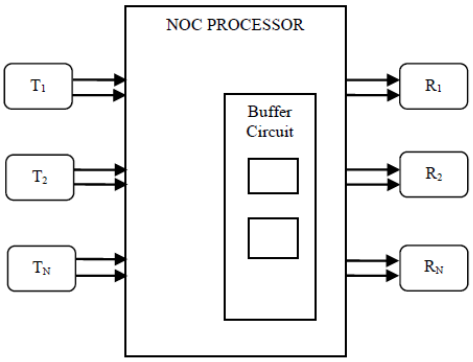

Figure 2 Buffered Routing

A. *Automated Test Equipment Tool*

Automatic or Automated Test Equipment (ATE) is any apparatus that performs tests on a device, known as the Device Under Test(DUT), using automation to quickly perform measurements and evaluate the test results. An ATE can be a simple computer controlled digital millimeter, or a complicated system containing dozens of complex test instruments (real or simulated electronic test equipment) capable of automatically testing and diagnosing faults in sophisticated electronic packaged parts or on Wafer testing, including System on chip and Integrated circuits.

B. Unicast based Multicast Method

A unicast-based multicast scheme completes multicast by using multiple unicast steps, therefore, it is not necessary to modify the unicast router architecture. Figure shows

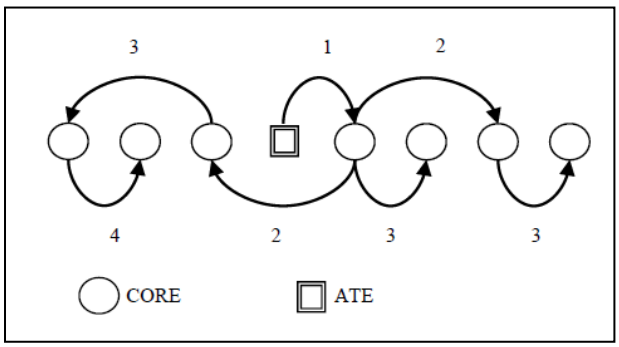

Figure 3 Unicast Based Multicast

All cores have different data rate for that buffers are used to deliver the data. By removing the buffers the sender sends the request to the receiver whether it has same data rate. If it not, the receiver sends the data rate to the sender and deliver the data.

C. Test Data Delivery Algorithm

A test packet is deliver to v_i ($1 \leq i \leq 8$) where all destinations and the source connected to the ATE are arranged as a dimension ordered chain. The dimension drder chain is divided into two equal parts D1 and D2. Cores deliver the test packet to D1 and D2 in bufferless routing, for that the frequency must be synchronized and deliver the packet based on the algorithm. Figure 4 and 5 shows the data deliver.

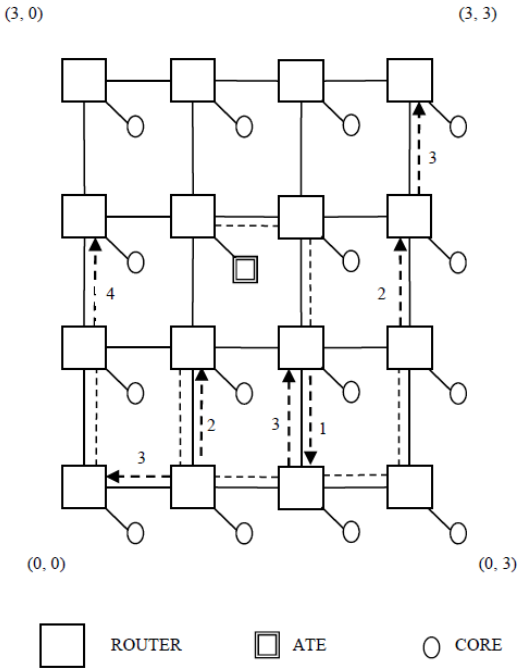

Figure 4 Test Data Deliver in NoC

Figure 4 and 5 shows the cores are arranged in dimension order chain and data are delivered by using unicast based multicast scheme.

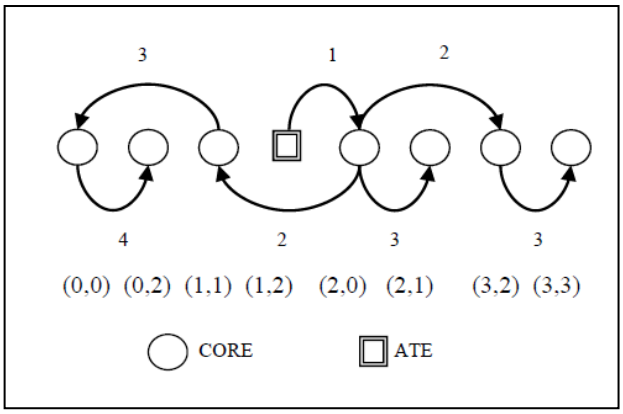

Figure 5 Test Data Deliver

Input:

Several numbers of cores

Output:

Data deliver to several numbers of cores

STEPS

1. The test vectors are arranged in dimension order (D).
2. The core (c) sequence divided into equal parts D1 and D2
3. Let c be the lower half of D1

   a.) While deliver the test packet for bufferless routing, synchronize the frequency and send to first node to D1.

   b.) Otherwise deliver the test packet for bufferless routing, synchronize the frequency and send to second node in D2.

4. Let c be the upper half of D2

   a.) While deliver the test packet for bufferless routing, synchronize the frequency and send to last node in D1.

   b.) Otherwise deliver the test packet for bufferless routing, synchronize the frequency and send to before last node in D2.

D. Test Response Collection Algorithm

The Test response collection graph use Y-X routing. The successors of a node become its predecessors, where the unique predecessor of an each node in the multicast tree becomes its unique successor. Test response of each test vector in a core is sent back to the node connected to the ATE as a single response packet. Figure 6 and 7 shows the response collection method of delivered data.

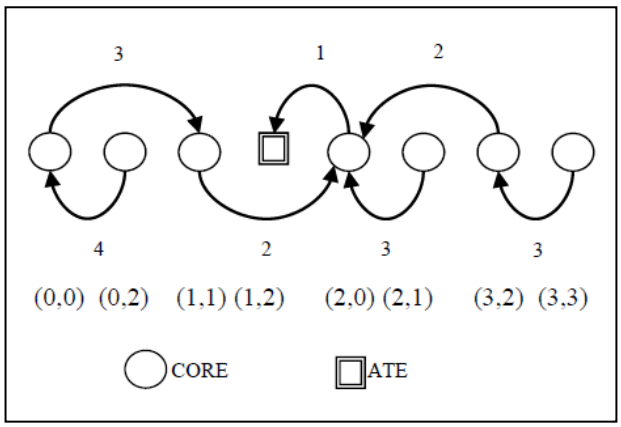

Figure 6 Test Response Collection

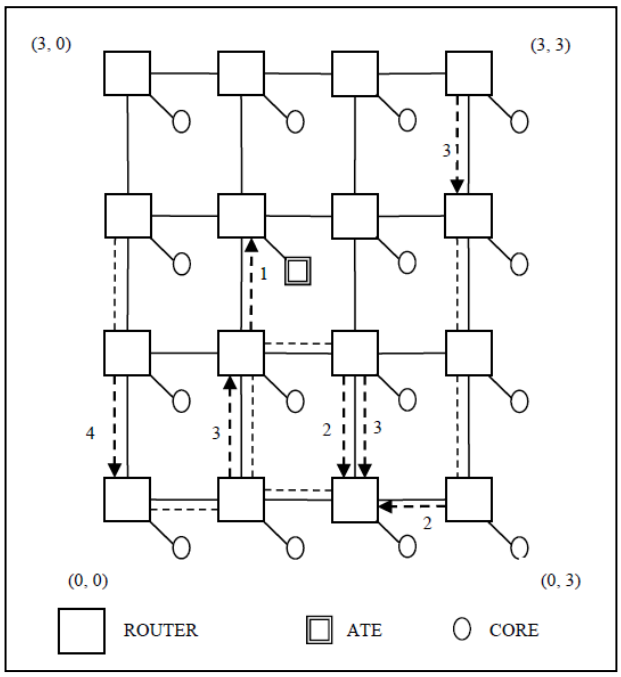

Figure 7 Test Response Collection in NoC

V. CONCLUSION

A new NoC core testing scheme was proposed using a new unicast based multicast scheme and bufferless routing. Test generation for all cores in the on-chip network can be completed by merging all cores into a single circuit, according to which test stimulus data volume can be reduced significantly that was formulated into a unicast based multicast problem. By eliminating the buffer we can significantly reduce the power.

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Characteristic Based Modelling Approach for Embedded Electronics using Object Modelling Technology

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Abstract : Embedded systems are of modern day interest to the fast growing IT Sector. Embedded systems are specifically designed to do somespecific task, as against general systems are designed for performing multiple tasks. Certain systems also have real-time performance constraints for reasons such as safety and usability; others may have low or no performance requirements, allowing the system hardware to be simplified to reduce costs. Embedded systems range from no user interface at all dedicated only to one task to complex graphical user interfaces that resemble modern computer desktop operating systems. The paper proposes a set of diagrams based on object orientation principle which describes hardware and software functionalities. The diagrams depicts the functional, behavioral and structural aspects of the embedded electronics system. The proposed modeling methodology is based on the principle of object orientation, which allows describing both software and functionalities explicitly. Furthermore, it is illustrated how the well-known object-oriented specification language unified modeling language can be adopted, to provided an adequate formalization of its semantics, to describe structural and behavioral aspects of smart phone database management system related to both logical and physical parts. It is needed to implement the software on the basis of Object Oriented Model developed. Flaw in modeling process can substantially contribute to the development cost and time. The operational efficiency may be affected as well. Here special attention is paid in planning phase and the same is extended to the implementation phase of the paper.

I. INTRODUCTION

Modeling is a process used to define and analyze data requirements needed to support the business processes within the scope of corresponding information systems in organizations. Therefore, the process of data modeling involves professional data modelers working closely with business stakeholders, as well as potential users of the information system. There are three different types of data models produced while progressing from requirements to the actual database to be used for the information system. The data requirements are initially recorded as a conceptual data model which is essentially a set of technology independent specifications about the data and is used to discuss initial requirements with the business stakeholders. The conceptual model is then translated into a logical data model, which documents structures of the data that can be implemented in databases. Implementation of one conceptual data model may require multiple logical data models. The last step in data modeling is transforming the logical data model to a physical data model that organizes the data into tables, and accounts for access, performance and storage details. Data modeling defines not just data elements, but their structures and relationships between them. Data modeling techniques and methodologies are used to model data in a standard, consistent, predictable manner in order to manage it as a resource. The use of data modeling standards is strongly recommended for all projects requiring a standard means of defining and analyzing data within an organization, e.g., using data modeling:

- to manage data as a resource;
- for the integration of information systems;
- for designing databases/data warehouses (aka data repositories)

Data modeling may be performed during various types of projects and in multiple phases of projects. Data models are progressive; there is no such thing as the final data model for a business or application. Instead a data model should be considered a living document that will change in response to a changing business. The data models should ideally be stored in a repository so that they can be retrieved, expanded, and edited over time. Whitten (2004) determined two types of data modeling:

- Strategic data modeling: This is part of the creation of an information systems strategy, which defines an overall vision and architecture for information systems is defined. Information engineering is a methodology that embraces this approach.
- Data modeling during systems analysis: In systems analysis logical data models are created as part of the development of new databases.

Data modeling is also used as a technique for detailing business requirements for specific databases. It is sometimes

called *database modeling* because a data model is eventually implemented in a database.

UML is an industry standard modeling notation, which provides foundational benefits:

- We have the potential of handing your diagram to someone who already knows how to interpret the notation without being told.
- We (and our audience) can find books, training, articles, web sites, and other educational and support resources for UML.
- There has been widespread tool adoption of UML, from drawing tool templates to repository based modeling tools to integrated development environments.
- We and many of your stakeholders can increase personal market value by mastering the notation we can hire people who know how to read and write UML diagrams without requiring training.

UML is a very structured notation. The specific structure brings benefits:

- The precise structure of the diagrams assists with consistency, completeness, and scope. Recasting your architectural vision into a predefined structure forces you to ask the right questions and flesh out the appropriate details.
- The fact that it is a structured notation makes it possible for tool vendors to provide functionality to transform a diagram from one view to another or even to code.

Static analysis aims at recovering the structure of a software system, while dynamic analysis focuses on its run time behavior. We propose a technique for combining the analysis of static and dynamic architectural information to support the task of architecture reconstruction. The approach emphasizes the correct choice of architecturally significant concepts for the reconstruction process and relies on abstraction techniques for their manipulation. The technique allows the software architect to create a set of architectural views valuable for the architecture description of the system.

To support our technique, we outline an environment that relies on hierarchical typed directed graphs to show the system's structure and message sequence charts for its behavior. The main features of the environment are: visualization of static and dynamic views, synchronization of abstractions performed on the views, scripting support and management of the use cases.

II. USE CASE DIAGRAM

- **Use cases**. A use case describes a sequence of actions that provide something of measurable value to an actor and is drawn as a horizontal ellipse.
- **Actors**. An actor is a person, organization, or external system that plays a role in one or more interactions with your system. Actors are drawn as stick figures.
- **Associations**. Associations between actors and use cases are indicated in use case diagrams by solid lines. An association exists whenever an actor is involved with an interaction described by a use case.

Associations are modeled as lines connecting use cases and actors to one another, with an optional arrowhead on one end of the line. The arrowhead is often used to indicating the direction of the initial invocation of the relationship or to indicate the primary actor within the use case. The arrowheads are typically confused with data flow and as a result I avoid their use.

- **System boundary boxes (optional)**. You can draw a rectangle around the use cases, called the system boundary box, to indicates the scope of your system. Anything within the box represents functionality that is in scope and anything outside the box is not. System boundary boxes are rarely used, although on occasion I have used them to identify which use cases will be delivered in each major release of a system.
- **Packages (optional)**. Packages are UML constructs that enable you to organize model elements (such as use cases) into groups. Packages are depicted as file folders and can be used on any of the UML diagrams, including both use case diagrams and class diagrams. I use packages only when my diagrams become unwieldy, which generally implies they cannot be printed on a single page, to organize a large diagram into smaller ones
- **Include**: **Include** is like a reference to next part, the use case is not completed without it. This part should be referenced from more places otherwise its use has no sense. An including use case calls or invokes the included one. Inclusion is used to show how a use case breaks into smaller steps. The included use case is at the arrowhead end.
- **Extend**: An extending use case adds goals and steps to the extended use case. The extensions operate only under certain conditions. The extended use case is at the arrowhead end.

Importance of Use cases:

- Use cases are important because they are in a tracking format. Hence they make it easy to comprehend about the functional requirements in the system and also make it easy to identify the various interactions between the users and the systems within an environment. They are descriptive and hence clearly represent the value of an interaction between actors and the system. They clarify system requirements very categorically and systemically making it easier to understand the system and its interactions with the users. During the analysis phase of the project's System Development Life Cycle, use cases help to understand the system's functionality.

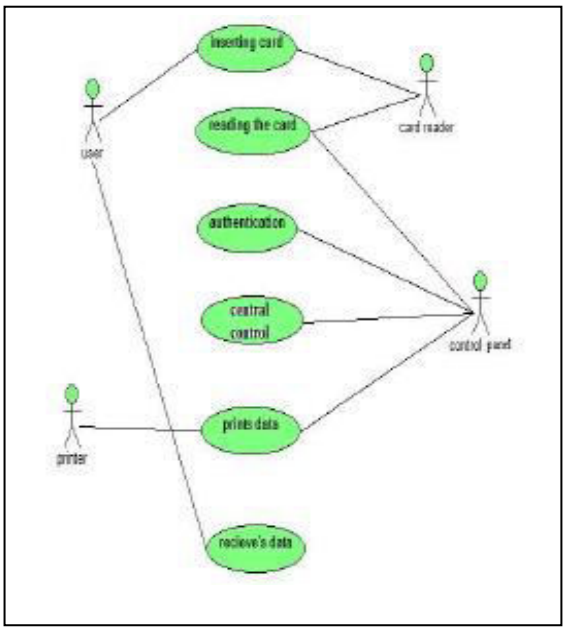


Fig.1 Use case diagram for ATM:

The above use case diagram gives the over view of operation of automatic teller machine .Here we have three actors namely User, Printer, Card reader and Control panel. The entire operation is describe in the use case diagram .The user inserts the card in the ATM system when the card is inserted by the user the data is read by the card reader .The control panel controls the entire system. Then authentication process takes place that weather user and password matches or not .If the user need the account bill it can be printed by printer.

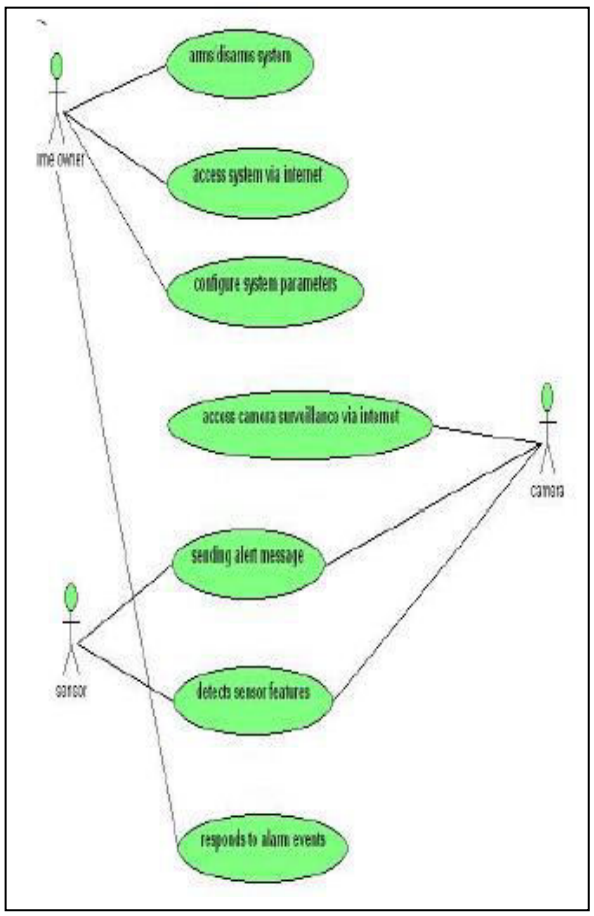


Fig.2 use case for home security systems

The above figure explains the use case diagram of home security system here we define three actors namely home owner, camera and sensor. It describe about to set the system to monitor sensor via camera with alarm when the home owner leaves the house or remains inside. System has been programmed for a password and to recognize various sensor the home owner arms and disarm system as required. He/she access the entire system via internet so that the home owner can be alert regarding his some security when he\she leaves the house or remains inside. The sensor if detects something unusual it sends the information to the camera. So that the features of information are detected by camera. With alarm the alert messages sent to the home owner that he responds to the alarm event.

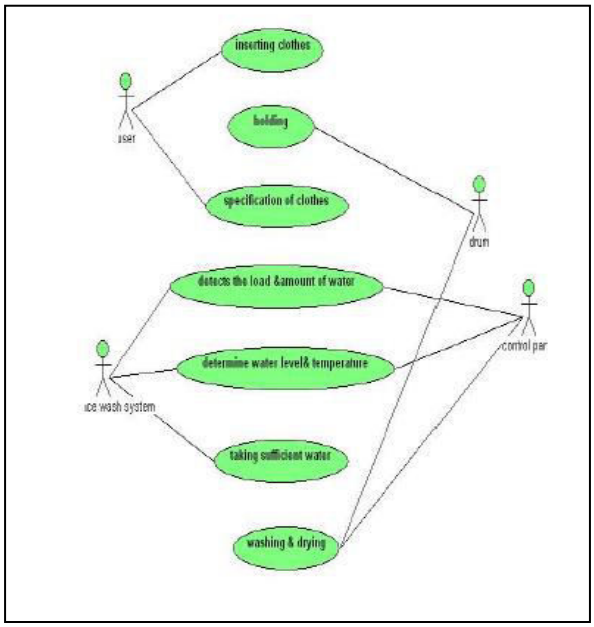


Fig.3 Use case diagram for washing machine

The above use case diagram gives the overview of operations that are done interior of washing machine. The actors here are user, drum, intelligence wash system, control panel. The clothes are inserted by the user as the cloths inserted have been hold by drum. The user should specify the type of clothes (whether cotton, or silk, etc...). After the specification the intelligence wash system as it has been programmed, automatically it detects the load and amount of water. And temperature the detergent are determine by intelligence wash system. The control panel control overall operation. The washing and drying is then done automatically.

III. INTERACTION DIAGRAM

Once the use cases are specified, and some of the core objects in the system are prototyped on class diagrams, we can start designing the dynamic behavior of the system.

Diagram Elements:

- Object. Each of the objects that participate in the processing represented in the sequence diagram is drawn across the top. Note that objects are used in this diagram while classes are used in use cases, class diagrams, and state-transition diagrams.
- Lifeline. A dotted line is dropped from each object in the sequence diagram. Arrows terminating on the lifeline indicate messages (commands) sent to the object. Arrows originating on the lifeline indicate messages sent from this object to another object. Time flows from top to bottom on a sequence diagram. Active. To indicate that an object is executing, i.e., it has control of the CPU, the lifeline is drawn as a thin rectangle.
- Message. A horizontal arrow represents a message (command) sent from one object to another. Note that parameters can be passed as part of the message and can (optionally) be noted on the diagram.
- Return. When one object commands another, a value is often returned. This may be a value computed by the object as a result of the command or a return code indicating whether the object completed processing the command successfully. These returned values are generally not indicated on a sequence diagram; they are simply assumed. In some instances the object may not be able to return this information immediately. In this case, the return of this information is noted on the diagram later using a dotted arrow. This indicates the flow of information was based on a previous request.
- Conditional. Square brackets are used to indicate a conditional, i.e., a Boolean expression that evaluates to TRUE or FALSE. The message is sent only if the expression is TRUE.
- Iteration. Square brackets preceded by an asterisk (*) indicate iteration. The message is sent multiple times. The expression within the brackets describes the iteration rule.
- Deletion . An X is used to indicate the termination (deletion) of an object.

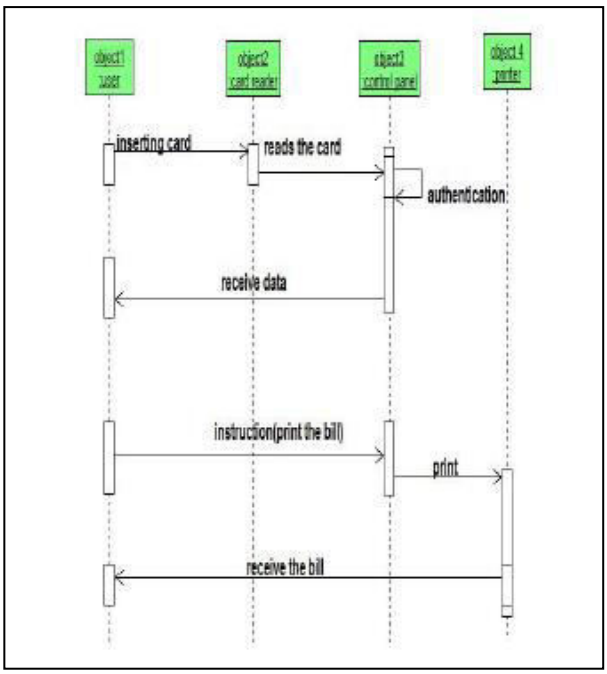


Fig. 4 Sequence diagram for ATM:

The sequential operation of automatic teller machine can be overviewed above .The user initially inserts the card .the data is then read by card reader .It determines whether the user's name matches the user password .if so the process authentication responds to user .if the user needs the bill (e.g. mini statement) it is printed by the printer.

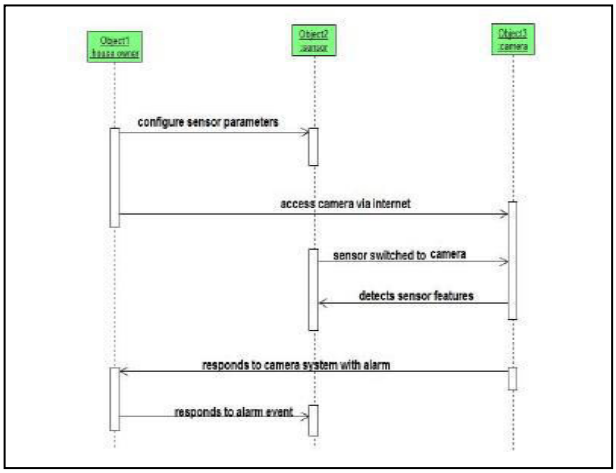
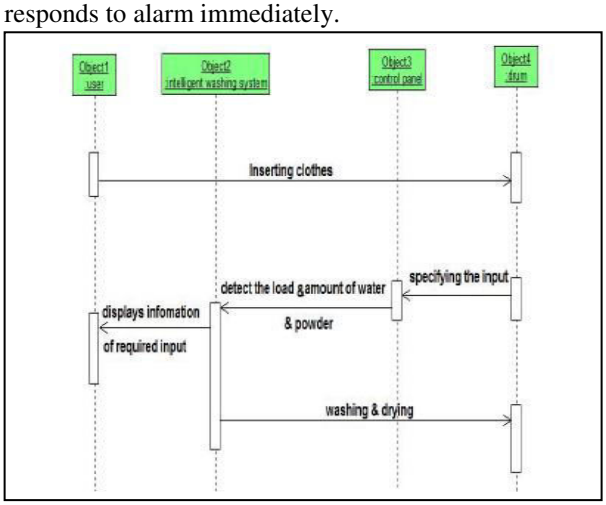


Fig.5 Sequence diagram of home security system

Here the above figure describe about the sequence action of actors during the operation of home security system. The object mentioned here is three namely homeowner, sensor, camera. It describes about the sequence activity of these three actors. The first step of the home owner is configuring sensor parameters and then camera which is accessed via internet.

The sensor then switches to camera if any unusual are defected. As soon as the information reaches the camera it detects the features of information that sent by sensor and sends the information to the home owner about the information with alarm. The home owner may responds to alarm immediately.



The above sequence diagram defines the overview of sequential activity for operation of washing machine. Here we have objects / actor such as user, intelligent washing system, control panel and drum. The user inserts the clothes and drum holds it. Then user should specify the input. After determining the type of clothes, the load and amount of water are determined by intelligence wash system and automatically washing and drying is done by it. The control panel does the entire control system of machine.

IV. ACTIVITY DIAGRAM

Activity diagrams are typically used for business process modeling, for modeling the logic captured by a single use case or usage scenario, or for modeling the detailed logic of a business rule. Although UML activity diagrams could potentially model the internal logic of a complex operation it would be far better to simply rewrite the operation so that it is simple enough that you don't require an activity diagram. In many ways UML activity diagrams are the object-oriented equivalent of flow charts and data flow diagrams (DFDs) from structured development

- **Initial node**. The filled in circle is the starting point of the diagram. An initial node isn't required although it does make it significantly easier to read the diagram.
- **Activity final node**. The filled circle with a border is the ending point. An activity diagram can have zero or more activity final nodes.
- **Activity**. The rounded rectangles represent activities that occur. An activity may be physical, such as Inspect Forms, or electronic, such as Display Create Student Screen.
- **Flow/edge**. The arrows on the diagram. Although there is a subtle difference between flows and edges I have never seen a practical purpose for the difference although I have no doubt one exists. I'll use the term flow.
- **Fork**. A black bar with one flow going into it andseveral leaving it. This denotes the beginning of parallel activity.
- **Join**. A black bar with several flows entering it and one leaving it. All flows going into the join must reach it before processing may continue. This denotes the end of parallel processing.
- **Condition**. Text such as [Incorrect Form] on a flow, defining a guard which must evaluate to true in order to traverse the node.
- **Decision**. A diamond with one flow entering and several leaving. The flows leaving include

conditions although some modelers will not indicate the conditions if it is obvious.

- **Merge**. A diamond with several flows entering and one leaving. The implication is that one or more incoming flows must reach this point until processing continues, based on any guards on the outgoing flow.
- **Partition**. It is organized into three partitions, also called swim lanes, indicating who/what is performing the activities (Either the Applicant, Registrar, or System).
- **Sub-activity indicator**. The rake in the bottom corner of an activity, such as in the Apply to University activity, indicates that the activity is described by a more finely detailed activity diagram. In this the Enroll in Seminar activity includes this symbol.
- **Flow final**. The circle with the X through it. This indicates that the process stops at this point.

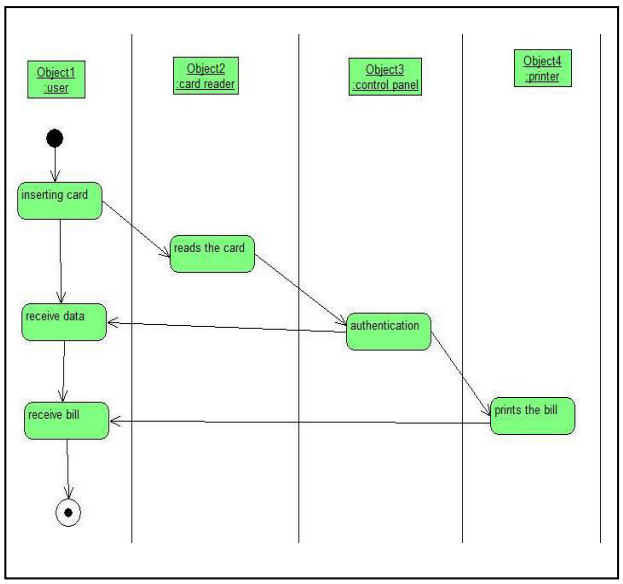


Fig.7 Activity diagram for ATM

The user inserts the card and mention the required data that needed by the system .Then after that conformation of the user, he/she can able to check the account information or any information he/she required .the bill can also be received if required by the user from the system. The card reader reads the card, then authentication process goes on determining user specification .if the user specifies regarding his account balance to be specified, then the bill is printed by the printer.

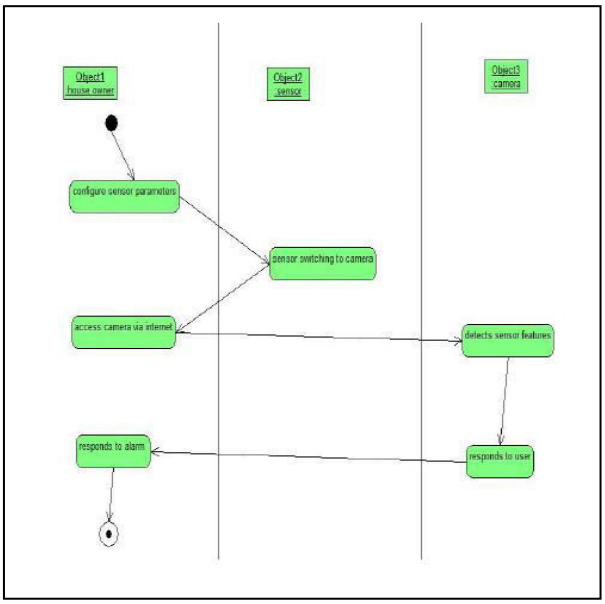


Fig.8 Activity diagram for home security system

The above figure describe about the activity performed by each member/actors/object in the system. As we seen before there are three actors /object. Namely home owner, sensor, camera. The home owner initially configures system parameters. He / She configure the entire system. The camera which is one of the actor is accessed via internet by the house owner. During emergency the alarm alerts the house owner and he/she response to it. The sensor when detects. Something unusual switches to camera. The camera detects the information features sent by sensor and sends the message to home owner with alarm which gives security for home .

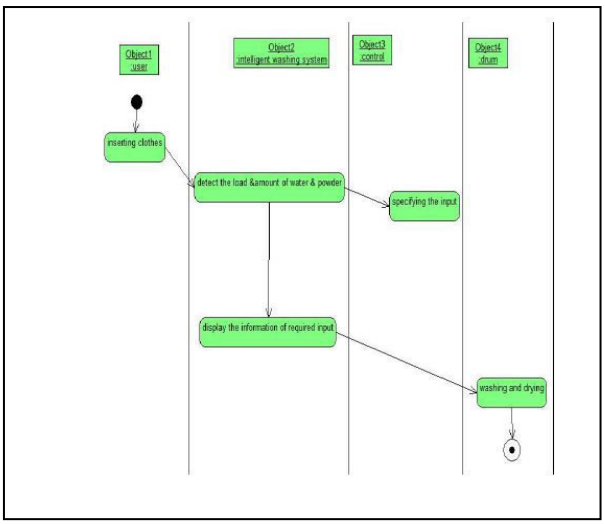


Fig.9 Activity diagram for washing machine

The user inserts the clothes and specifies the type of cloth. Then the operation of determining the amount of water and powder, display the information of required input, washing and drying are controlled and performed sequentially by intelligence wash system.

ACKNOWLEDGEMENT

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Automatic Generation Control of Multi Area Power System with Extended PI and Fuzzy Logic Controller Considering Nonlinearities

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Abstract - This paper describes the Load Frequency Control (LFC) of interconnected reheat thermal system using Extended Proportional - Integral (EPI) and Fuzzy Logic Controller (FLC). The extended PI controller is used to reduce the peak over shoot and settling time error in the past. The action of this controller provides satisfactory operation when compared to the PI scheme even with the consideration of singularities of speed governor such as rate limit on valve position. This extended PI controller is greatly dependent on the decaying factor. The value of decaying factor should be carefully chosen otherwise it greatly affects the control performance. To overcome this drawback Fuzzy Logic Controller has been employed in the system. The aim of the FLC is to restore the frequency in a very smooth way to its nominal value in the shortest possible time, if any load change occurs. The performance of FLC has been compared with extended PI control both in the presence and absenceof nonlinearities namely governor dead band and generation rate constraint. System performance is examined considering 1% step load perturbation in either area of the system.

Keywords- *Area Control Error (ACE); Fuzzy Logic Controller (FLC); Generation rate constraint (GRC); Governor Dead Band (GDB); Load Frequency Control (LFC); Proportional-Integral (PI).*

I. INTRODUCTION

In electric power generation, system disturbances due to load fluctuations tend to variation in desired frequency value. Automatic Generation Control (AGC) or Load Frequency Control is a very important issue in power system operation and control for supplying sufficient and reliable electric power with good quality. An interconnected power system can be considered as being divided into control areas, which are connected by the tie lines. In each control area, all generators are assumed to form a coherent group. The power system is subjected to local variations of random magnitude and duration. For satisfactory operation of a power system the frequency should remain nearly constant. The frequency of a system depends on active power balance. As frequency is a common factor throughout the system, a change in active power demand at one point is reflected throughout the system. Many investigations have been reported in the past pertaining to LFC of a multi area interconnected power system [1]. In the literature, some control strategies have been proposed based on classical control theory. Due to unnecessary errors in the past, the conventional PI control scheme does not provide adequate control performance with the presence of non-linearity. This paper develops an extended PI control to the LFC scheme with the consideration of nonlinearities such as governor dead band and generation rate constraint in order to get rid of the overshoot of the conventional PI controller. The basic idea of this proposed controller is decaying factor, which reduces the effects of the error in the past. For an optimal or near optimal performance, it is necessary that the decaying factor as well as the feedback gain should be changed very quickly in response to change in the system dynamics. However due to inherent characteristics of changing load and the system non-linearities it is very difficult to obtain the optimum value of decaying factor [2]. The difficulty in obtaining the optimum settling time of previously said controller is mitigated by using FLC, which gives the opportunity to describe the control action in qualitative term and symbolic form.

Literature survey shows that [3], only a few investigations have been carried out using FLC to LFC. It has been discussed that the implementation of such FLC has greatly improved the performance of the controller "without negatively affecting the consumers' quality of supply". This paper addresses the comparison between the performances of FLC and extended PI controller, both in the presence and absence of non-linearities. The transfer function model of two area interconnected reheat thermal system is shown in the Fig.1.

II. SYSTEM INVESTIGATED

System investigation has been carried out on a two equal area reheat thermal power system considering GDB & GRC.The nominal parameters of the system are given in appendix. Mat lab version 7.9 has been used to obtain dynamic response of change in frequencies ΔF_1, ΔF_2 and change in tie line ΔPtie for 1% step load perturbation. The system has been designed for nominal frequency. Proper assumptions and approximations are made to linearize the mathematical equations which describe the system and transfer function model [3] [4].

A. Governor dead band

GDB is defined as the total magnitude of a sustained speed change within which there is no resulting change in valve position [7]. Describing function approach is used to incorporate the governor dead band nonlinearity. The hysteresis type of nonlinearity is expressed as

Y=F(x, x˙) rather than as y=F(x) --- (1)

Where, A is amplitude of oscillation

$\omega\circ$ is frequency of oscillations

$\omega\circ = 2\pi fo$ ---(2)

As the variable function is complex and periodic function of time, it can be developed in fourierseries as follows [8]

$$F(x,\dot{x}) = 0.8x - 0.2\dot{x}/_{\pi}$$

--- (3)

B. Generation rate constraint

In practice there exists a maximum limit on the rate of change in a generating power. For thermal system a generating rate limitation of 0.1p.u per minute is considered.

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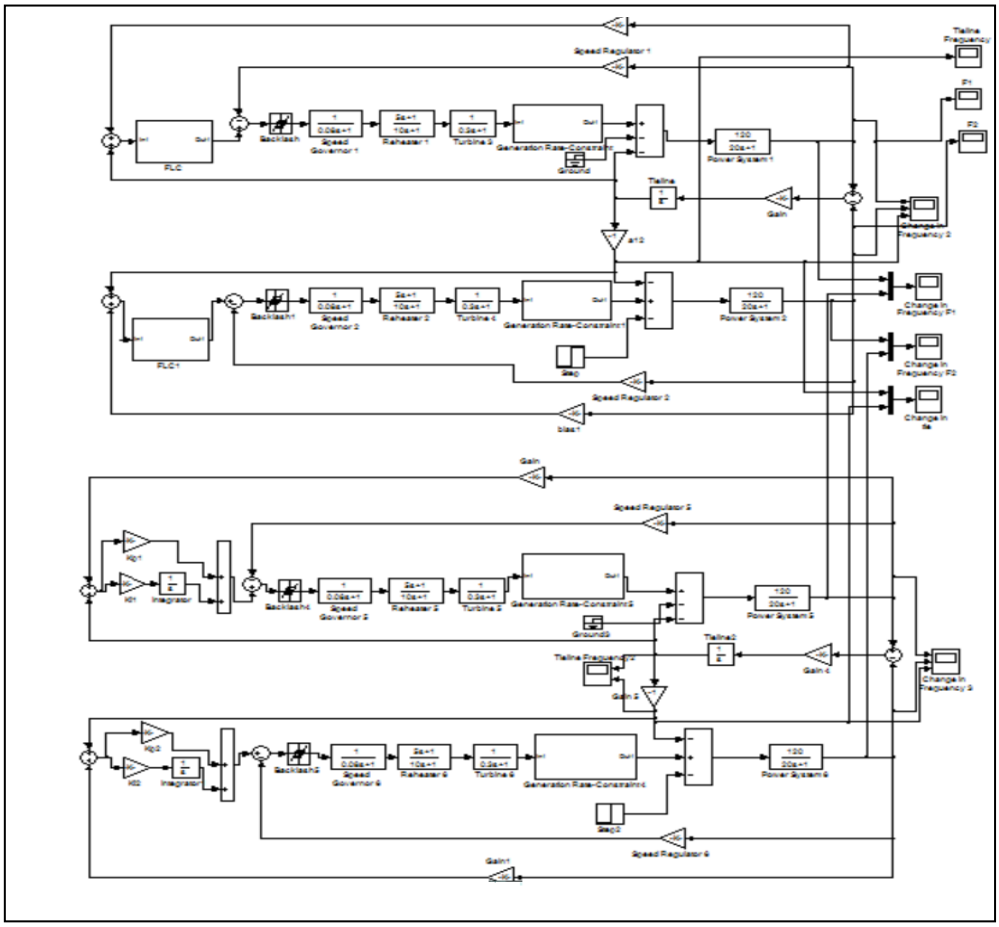

Fig. 1. Transfer Function Model of Two area Thermal Interconnected System

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Rate limits are imposed to avoid variation in process like temperature and pressure for the safety of equipment [6].

The main reason to consider to the GRC is that the rapid power increase would draw out excessive steam from the boiler system to cause steam condensation due to adiabatic expansion. The condensation of steam may produce minute water drops to abrade the turbine blade by hitting. The steam valve of the high pressure turbine acts as a control valve associated with the LFC. Since the temperature and pressure in the HP turbine are normally very high with some margin, it is expected that the steam condensation would not occur with about 20% steam flow change unless the boiler steam pressure itself does not drop below a certain level. Block diagram of GRC is shown in fig 2.

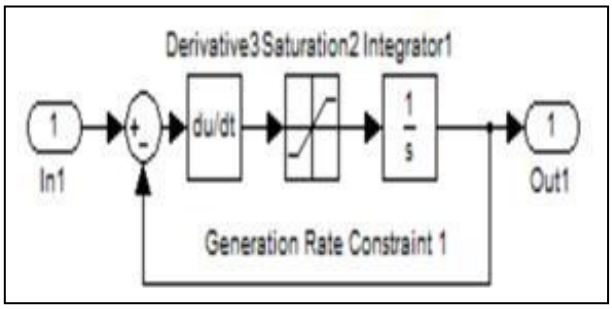

Fig 2. Block diagram of generation rate constraint

The long time abrasion of the turbine blade due to minute water drops can be serious problem while short time abrasion given little effects as the turbine blade. The boiler can afford to keep its steam pressure to be constant for a while, and thus it is possible to increase generation power up to certain limit of normal power during the first tens of seconds. After the generation power has reached this marginal upper bound the power increases of the turbine should be restricted by the GRC.

C. Conventional Extended PI Controller

The extended PI term is substituted for general PI term in conventional scheme. Performance index curve is sown in fig. 3, by which the value of PI controller is chosen. In EPI control scheme an exponential decaying function (λ) is chosen as follows,

$$h(t) = e^{-\lambda t}\, u(t) \qquad (4)$$

The extended integral control is given by,

$$\int_0^t e^{-\lambda(t-\tau)} \Delta f(\tau) d\tau \qquad (5)$$

with its s-domain function of $\frac{1}{(s+\lambda)}$

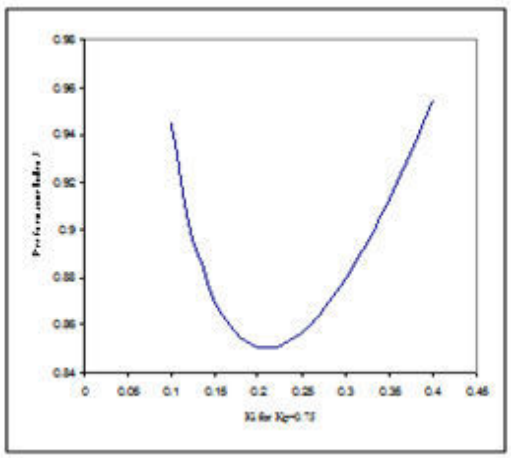

Fig 3. Performance index curve

The decaying factor of extended PI varies in proportion to the degree of deviation of feedback signals. For large overshoot, large value of decaying factor should be selected to reduce the effects of the error, while small decaying factor for small error [2][10].

III FUZZY LOGIC CONTROLLER

The concept of fuzzy logic was developed by Lotfi.A.Zadeh in 1965 to address uncertainty and imprecision which widely exists in engineering problems [5].The design of FLC can be normally divided into three areas namely allocation of area of inputs, determination of rules and defuzzifying of output into a real value [9]. In this paper the proposed fuzzy controller takes the input as ACE and ACĖ, which is given as,

$$ACE_i = \Delta F_i B_i + \Delta P_{tie_i} \qquad (6)$$

The Block diagram of Fuzzy Logic Controller is shown in Fig.4. Seven Membership Functions (MF) have been used to explore the best settling time.

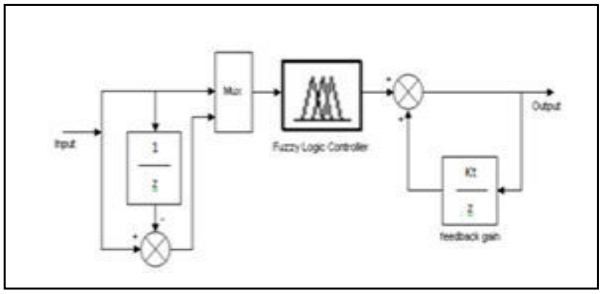

Fig 4. Fuzzy logic controller

MF specifies the degree to which a given input belongs to a set. Here seven membership functions namely Negative Big (NB), Negative medium (NM), Negative small (NS), Zero (ZO), Positive Small (PS), Positive medium (PM), Positive large(PL) are used.

Defuzzification to obtain crisp value of FLC output is done by center of area method. Fuzzy rules specify the relationship among the fuzzy variables. These rules help us to explain the control action in qualitative terms.

IV. SIMULATION RESULTS

The system is simulated for a step load disturbance of 1% on second area of the system. Due to this the change in dynamic response of the system has been observed both in the presence and absence of nonlinearities. Finally the simulation results of two-area system with FLC have been compared with extended PI control. FLC yields fast settling time with less number of oscillations which advocates the smooth settlement of the quality power supply. Fig 5a-5c shows the simulation result for the system without nonlinearities and fig 6a-6c shows the result for system with nonlinearities.

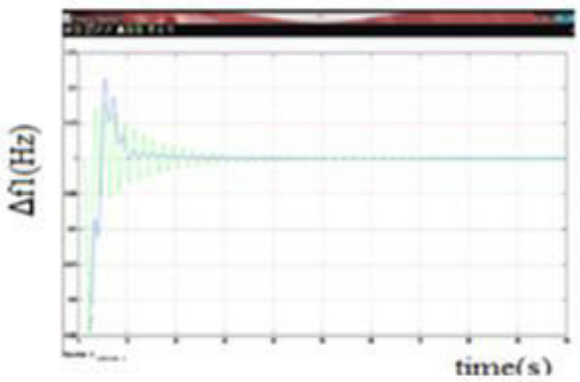

Fig. 5a. Change in frequency f1

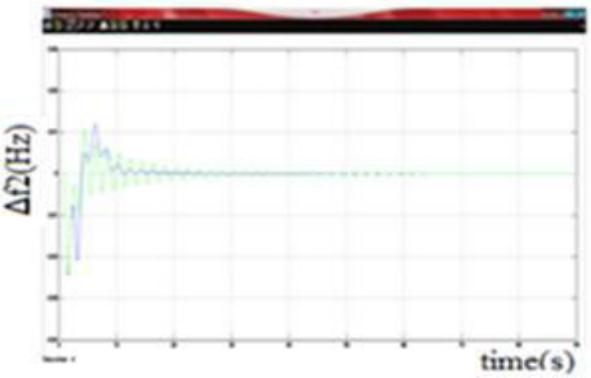

Fig 5b. Change in frequency f2

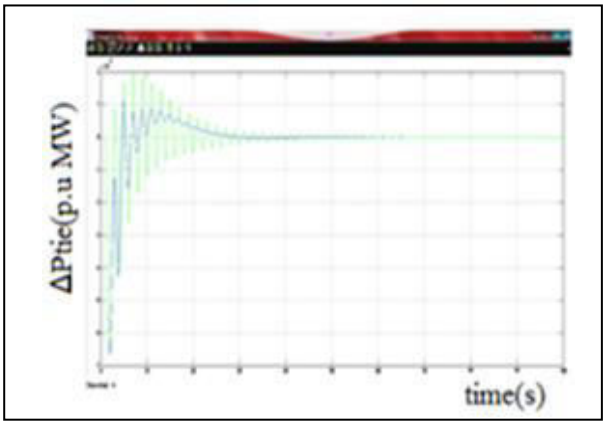

Fig 5c. change in tie line

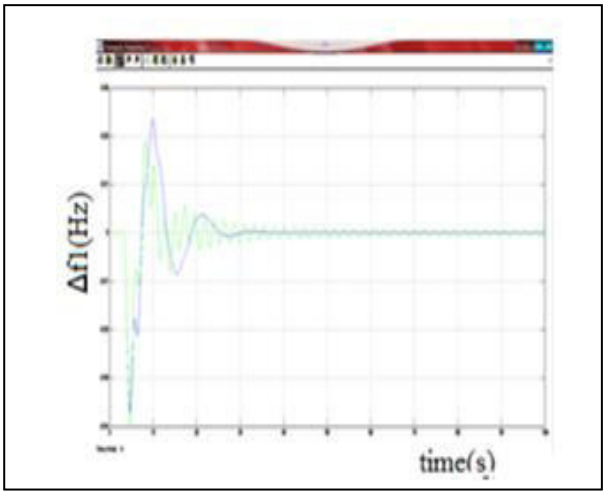

Fig. 6a. Change in frequency f1

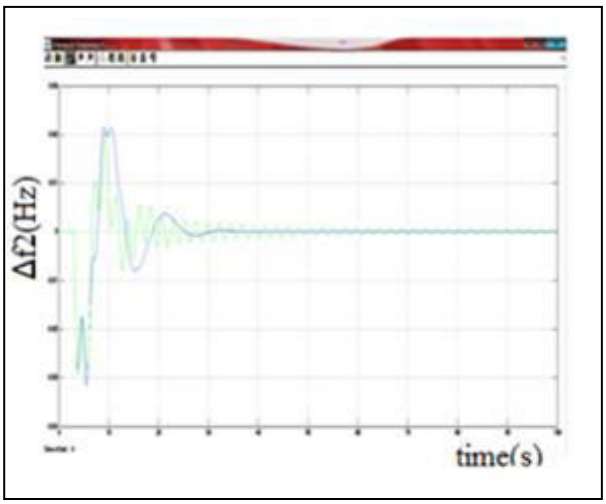

Fig 6b. Change in frequency f2

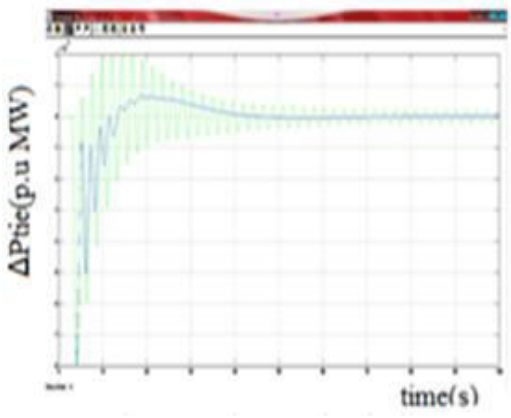

Fig 5c. change in tie line

V. CONCLUSION

In this paper FLC is designed for automatic load frequency control of two area interconnected power system. The system performance is observed on the basis of dynamic parameter (i.e.) settling time. The comparison of the dynamic responses of proposed controllers is shown in table 1. The simulation result shows that the FLC yields much improved control performance when compared to extended PI controller.

TABLE 1. COMPARISON STUDY OF SETTLING TIME

Non-Linearity	Controllers	Δf1	Δf2	ΔPtie
With GDB & GRC	Fuzzy	35 s	35 s	43 s
	Extended PI	-	-	-
Without GDB & GRC	Fuzzy	31s	34 s	44 s
	Extended PI	52 s	52 s	75 s

VI APPENDIX

P_{ri}=2000 MW T_{ti} =0.3s

T_{gi}=0.08s K_{ri}=0.5s

T_{ri}=10s K_{pi}=100 Hz/pu MW

T_{pi}=20 s T_{12}=0.086

R_i=2.4 Hz/ pu MW B_i =0.425 pu MW/Hz

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Design of PEF Treatment Chamber for Liquid Food Processing

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Abstract - The pulsed electric field technology (PEF) is a highly effective method and emerging new technology for liquid food preservation. Compared to thermal processing, the PEF process is considered more energy efficient as the microbial or enzymatic inactivation is achieved at ambient or mild temperatures by the application of pulsed electric field to liquid food flowing or placed in between two electrodes. High voltage pulses probably causes electroporation of the cell membranes resulting in the inactivation of microorganisms.

The key component of this technology is the treatment chamber, in which the food is exposed to pulsed electric field. In this work, PEF continuous flow treatment chamber design is studied using Finite Element Method (Maxwell Ansoft) and the field distribution is analyzed. From the analysis it can be observed that uniform electric field distribution is achieved across the effective treatment region in the treatment chamber. The design of treatment chamber, operational parameters, and their optimization for the process is given utmost importance. The design of Co-axial continuous flow treatment chamber model is fabricated for experimentation. Then experiment using static treatment chamber and continuous flow treatment chamber is done for preservation of tomato juice and the results are analyzed. It is suggested that pulse application of the order of about 25-kV/cm to 50-kV/cm electric field intensity be employed for the purpose of effective microbial reduction.

Keywords - *Electroporation, Co-axial continuous flow treatment chamber, PEF.*

I. INTRODUCTION

Heat pasteurization or sterilization of liquid foods is the traditional method used to inactivate spoilage microorganisms that might grow under conditions normally encountered in storage. However, during heat treatment the thermal degradation to the liquid food product can adversely affect the color, flavor, taste and its nutritional value causing irreversible loss of fresh flavor, aroma and its texture with initiation of undesirable browning reactions. Moreover, heat pasteurization is an energy intensive method. Due to these reasons, we go for non-thermal processing method such as high voltage pulsed electric field treatment which provides consumers with microbiologically safe and fresh quality foods without any loss of its quality and nutritional value.

There are several non-thermal pasteurization methods available in general. Among this High voltage pulsed electric field (PEF) treatment is the most promising non-thermal processing method that may radically change liquid food preservation technology. This method is been developed to achieve sufficient microbial reduction without much affecting the quality of food preserved. Applying PEF technology to food preservation offers high quality fresh-like liquid foods with excellent flavor, nutritional value, and shelf-life. Since it preserves foods without using heat, foods treated this way retain their fresh aroma, taste, and appearance.

The PEF treatment process involves the application of short pulse of high voltage electric field to foods flowing through or placed between two electrodes. The electric field may be applied in the form of exponentially decaying, square wave, bipolar, or oscillatory pulses and at ambient, sub-ambient, or slightly above-ambient temperature. The applied high voltage may probably cause electroporation of the cell membranes resulting in the inactivation of microorganisms.

II. TREATMENT CHAMBER

A PEF treatment occurs inside of a PEF treatment chamber, which houses electrodes and delivers a high voltage to a food material. Various types of PEF treatment chambers have been used for PEF treatments. The PEF treatment process may be either static or continuous. In the static processing, discrete portions of fluid food stuff are treated as a unit by subjecting all of the fluid to a PEF treatment chamber, in which uniform field strength substantially is applied to all elements of foodstuff to be treated and in the continuous processing, the food stuff is flowing into and emitted from the PEF treatment system in a steady stream by a pump and the

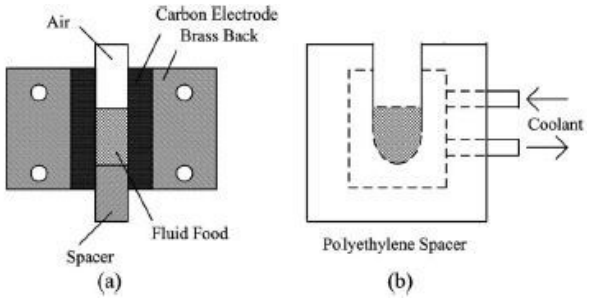
design of the treatment chamber is a gradual development from static treatment chambers to continuous treatment chambers.

A. Static Treatment Chambers

Static treatment chambers are mostly preferred in laboratory-scale experiments.

1) *U-Shaped Static Treatment Chamber*

This treatment chamber contains two carbon electrodes backed with brass blocks hollowed out for coolant flow with a U-shaped polythene spacer placed between the electrodes to form the chamber [fig 1]. Using this treatment chamber, the temperature rise of the suspension was small and did not cause the lethal effect. It was proposed that death of the organisms was not because of the products of electrolysis, but because of the electric field causing an irreversible loss of the membrane's function as the semi permeable barrier between the bacterial cell and its environment, ending in cell death. [Sale and Hamilton].



(a) Cut-away view showing the alignment of three parts.

(b) U-shaped spacer and coolant connection.

Fig. 1 : U-shaped static treatment chamber.

2) *Parallel plate Static Treatment Chamber*

In parallel plate static treatment chamber, the electrodes separated by an insulating spacer where uniform electric field strength can be achieved by parallel plate-electrodes with a gap sufficiently smaller than the electrode surface dimension. One apparent disadvantage in this design, however, is its inherent field strength limitation due to surface tracking on the fluid or insulator that leads to arcing.

A laboratory scale PEF treatment static test apparatus, designed is presented in Fig. 2 consisted of two substantially parallel stainless steel electrodes with a gap of 5 mm and an acrylic Plexiglas electrode spacer.

Treatment chambers with parallel plate-electrodes provide a uniform electrical field distribution along the gap axes and electrode surfaces, but it create a field enhancement problem at the edge of the electrodes. [Kang Huang, Jianping Wang]

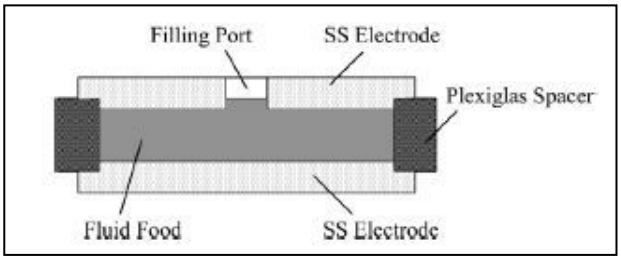


Fig. 2 : Parallel plate static treatment chamber

3) *Disk-Shaped Treatment Chamber*

It is important that the PEF treatment chamber should be designed to provide a high, relatively spatially uniform electric field in the treatment zone, while minimizing the capacity or conditions for electrical breakdown and is also important that the electrode surface should be designed to minimize field enhancement that increases the local electric field and results in electrical breakdown.

In this disk-shaped static chamber (Fig. 3) two round-edged disk-shaped stainless steel electrodes polished to mirror surfaces were held in position by insulting material that also formed an enclosure containing the food. Because the disk-shaped, round-edged electrodes minimized electric field enhancement and reduced the possibility of dielectric breakdown of the fluid foods and polysulfone or Plexiglas was selected as insulating materials. The appearance of space charge in the food would modify the electric field from the ideal no-space-charge situation. There was also a cooling system in this chamber, which was provided by circulating water at pre-selected temperatures through jackets built into the electrodes. [Qin et al].

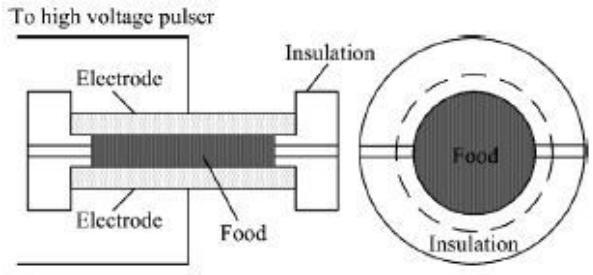


Fig. 3 : Disk-shaped static treatment chamber

4) *Glass Coil Static Chamber*

This model uses a glass coil surrounding the anode (Fig. 4). The volume of the chamber was 20 cm, which requires a filling liquid with high conductivity and similar permittivity to the sample (media NaCl solution, F = 0.8 to 1.3 S/m, filling liquid water ~ 10 S/m) used because there is no inactivation with a non-conductive medium (that is, transformer silicon oil).

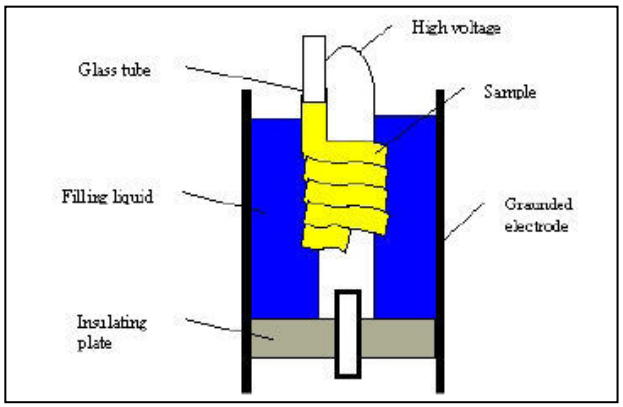


Fig. 4 : Static chamber with glass coil surrounding the anode.

B. Continuous Treatment Chambers

Coaxial and the cofield PEF treatment chambers are currently widely used due to their simplicity in structure [3]. Electrical current flows perpendicularly to food flow in coaxial PEF treatment chambers and in parallel to food flow in cofield flow PEF treatment chambers [1]. A cofield

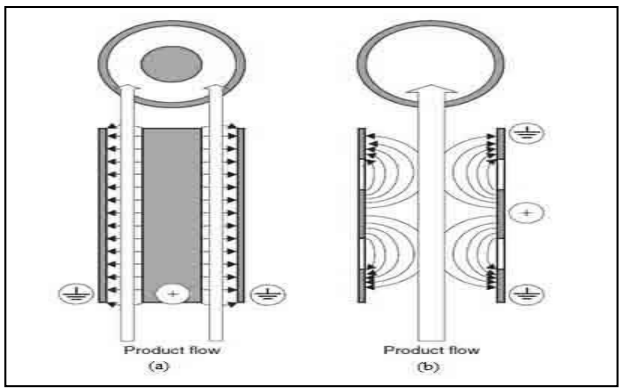


Fig. 5 (a).co axial chamber, (b)co field chamber

flow tubular PEF treatment chamber was invented by Yin *et al,* and used in commercial scale PEF systems [7], [8]. Schematic diagram of co axial and co field treatment chamber are illustrated in Fig.5

1) Co-axial Treatment Chamber:

Seacheol Min, Qin (1995) modified the coaxial treatment chamber design to provide a uniform electric field distribution as illustrated in Fig.6

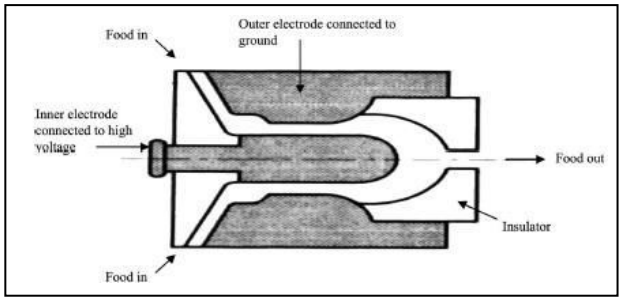


Fig. 6 : Modified co axial treatment chamber

Fig.7 illustrates the final electrode configuration in the treatment region.

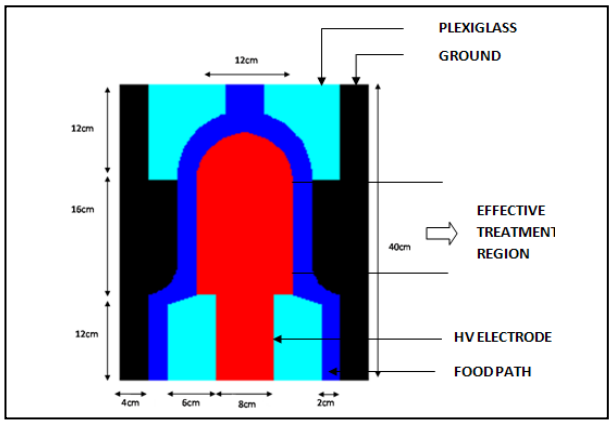


Fig. 7 : Electrode Configuration of Co-axial chamber

Electric field analysis for the effective treatment region can be analyzed by using ANSOFT simulation package. The electric field distribution for 40kV input voltage to the high voltage electrode is shown in Fig.8

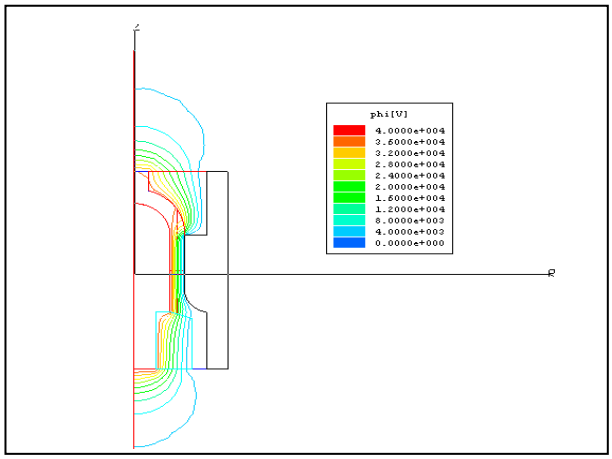


Fig.8 : Overall electric field distribution

Electric field distribution along x-axis for 50kV input voltage too the high voltage electrode is shown in Fig.9

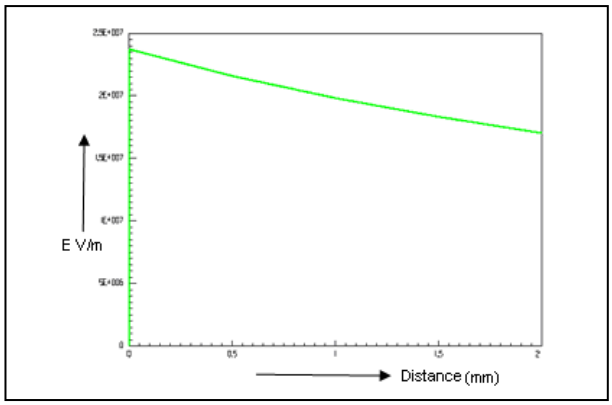


Fig.9 : Electric field distribution along X-axis

Simulation result shows Voltage is reducing linearly between the HV and ground electrode. In the effective treatment region, maximum electric field is measured at high voltage electrode 23.67kV/cm and minimum electric field is measured near to ground electrode as 16.98kV/cm. This implies in between the electric field inside the effective treatment region field is distributed evenly. These results can be verified with analytical calculation. For analytical calculation, cross sectional view of coaxial chamber effective treatment region was taken in to consideration as shown in fig.10

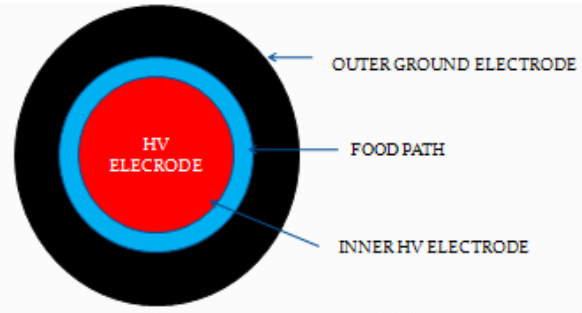


Fig.10 : Cross sectional view of Co-axial configuration for analytical studies.

$$E=V/(r*\ln(R2/R1)) \quad (2)$$

Where, R2-outer dia of electrode

R1-inner diameter of electrode

r-at a food path where we calculating electric field strength

The electric field strength in co-axial configuration is calculated using the above formulae. Analytical calculations is tabulated and compared with that simulation results as shown in table. 1.

Distance R(cm)	Measured value (kV/cm)	Analytical value (kV/cm)	Percentage error
6	23.39	23.67	0.28
6.5	21.37	21.615	0.245
7	19.56	19.813	0.253
7.5	18.04	18.199	0.259
8	16.75	16.98	0.23

Table.1 Comparison of analytical and simulation results

2) Co-Field Treatment Chamber

This chamber consists of a set of hollow, cylindrical electrodes separated by insulators, in which the product is pumped through the drilling. A cofield flow tubular PEF treatment chamber was invented by Yin *et al,* and used in commercial scale PEF systems [5]. Schematic diagram of co field treatment chamber is shown in Fig.9

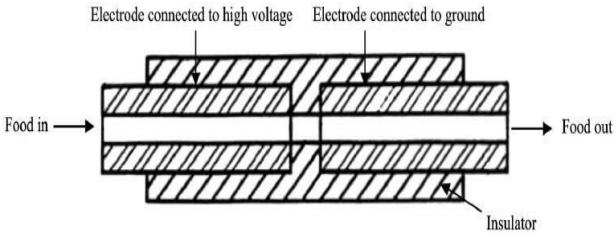


Fig.11: Schematic diagram of co-axial chamber

Co-field treatment chamber, the electric field is not constant. The distribution of the electric field in this type of chamber is variable depending on the exact configuration of the electrodes and to their relative position with respect to the insulating elements. A proper relationship to define the electric field intensity in the area between the electrodes has not been developed yet, thus Equation (3) is commonly employed.

$$E=V/d \quad (3)$$

The co-field treatment chamber includes three electrodes to supply the electric field to the food product. Each electrode includes an electrode flow chamber, allowing the flow of the food to be processed and the electrical contact with the food products. The electrodes are made in stainless steel with a cylindrical geometry. Each electrode includes an inlet and outlet opening to introduce the food material through the same electrodes in the axial direction. Thus, in this configuration the electric field lines are parallel. The electrode dimensions used in the co-field chamber which is studied is shown in Fig.11

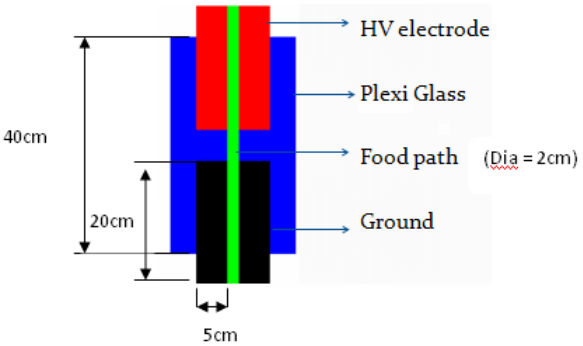


Fig. 12 : Electrode dimension of co field chamber

Electric field analysis for the effective treatment region can be analyzed by using ANSOFT simulation package. The electric field distribution for 0kV input voltage to the high voltage electrode is shown in Fig.11.

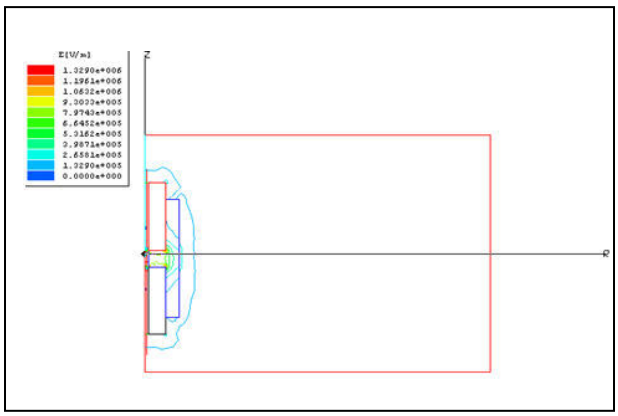


Fig.13 : Overall electric field distribution of co field chamber

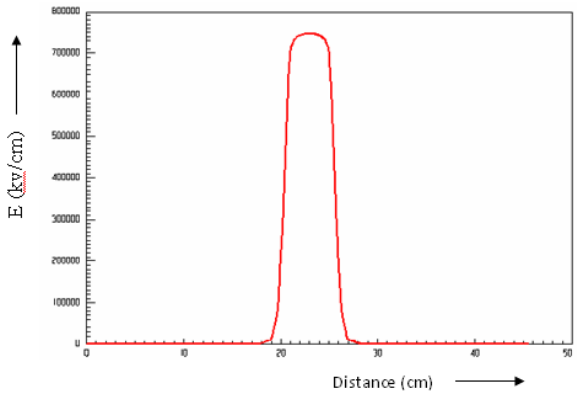


Fig.14 : E plot in vertical line along liquid food path with ε_r=79 and input voltage 40kV.

From the above graph, it can be seen that the electric field strength is only high at the effective treatment region of the treatment chamber. The electric field is uniformly distributed in the treatment region between the electrodes.

III. EXPERIMENTS AND RESULTS

To optimize the treatment voltage and pulse rate, treatment of tomato juice with static treatment chamber and continuous flow has been carried out. Tests are carried out with Impulse of (1.3/48 µsec), amplitude of 30kV, 50kV and various combinations, with 150pulse/90secs, 300pulse/180secs and various combinations. Chemical and Microbiological tests are carried out to study their outcome results before and after treatment and to find their shelf life extension. Tomato juice sample is prepared by adding 500ml of water with 500ml of pure tomato crush and 100 gm of sugar without adding any chemical reagents.

1) *Static Treatment Chamber*

Fig.15 : Static treatment Chamber

The experimental setup for the PEF treatment of liquid food processing using static chamber is shown in Fig 15. Modified Marx's generator is used to produce impulse voltages of (1.3/45 µsec). Experiment has been carried out to preserve tomato juice which is treated with test voltages and pulse rate of 30kV, 150 Pulses for 90 sec. 50kV, 150 Pulses for 90 sec, 50kV, 300 pulses for 180 sec. 50kV, 300 pulses (- ve impulse) for 240 sec. The treatment chamber is sterilized using Distilled water before and after carrying out experiments.

For existing properties various chemical test have been done on the treated sample and the results are tabulated in table. The treated samples were also subjected to microbial analysis to find shelf life extension of the tomato juice. This analysis is done to determine the reduction of microbial growth which is present in the juices.

Chemical and Microbial tests on controlled and treated samples were carried out in National Agro Foundation, Anna university campus, Taramani. to analyze existing properties and shelf life extension of the tomato juice and the results are tabulated as shown.

Table.2 Chemical test result for static processed.

SAMPLE	pH		ACIDITY		BRIX		VITAMIN C	
	1st day	7th day	1st day	7th day	1st day	7th day	1st day	7th day
Control	4.29	4.28	0.16	0.17	6	6	14.28	14.12
30kV, 150 Pulses	4.29	4.27	0.16	0.16	6	6	14.28	14.12
50kV, 150 Pulses	4.28	4.27	0.17	0.17	6	6	14.12	14.12
50kV,300 Pulses	4.29	4.28	0.17	0.17	6	6	14.12	14.04
50Kv, 300 Pulses (-ve)	4.27	4.29	0.17	0.18	6	6	14.12	14.04

Table.3 shows the microbiological test results

SAMPLE	MICROBIAL COUNT		% GROWTH
	1ST DAY	7TH DAY	
Control Sample	3450	5120	32
30kV, 150 Pulses	560	780	28
50kV, 150 Pulses	340	450	24
50kV,300 Pulses	280	340	18
50Kv, 300 Pulses (–ve)	260	310	16

From the above table, it is analyzed that pH, Acidity, Brix, Vitamin C values remains same in both controlled and treated samples with static treatment chamber. And effective microbial reduction is seen with applied PEF. This implies that the chemical properties and nutritional value does not vary when liquid food is subjected to PEF.

2) *Co-axial continuous flow treatment chamber.*

The experimental setup for the PEF treatment of liquid food processing is shown in Fig 16. Modified Marx's generator is used to produce impulse voltages of (1.3/45 µsec). Experiment has been carried out to preserve tomato juice which is treated with test voltages and pulse rate of 30kV, 150 Pulses for 90 sec. 50kV, 150 Pulses for 90 sec, 50kV, 300 pulses for 180 sec. 50kV, 300 pulses (- ve impulse) for 240 sec. Flow and the flow rate is adjusted using valve.

Fig.16: Co-axial Continuous flow treatment chamber.

Table. 3 : Chemical test result for continuous process.

SAMPLE	pH		ACIDITY		BRIX		VITAMIN C	
	1st day	7th day	1st day	7th day	1st day	7th day	1st day	7th day
Control	4.23	4.26	0.18	0.17	6	6	15.27	14.98
30kV, 150 Pulses	4.24	4.27	0.19	0.18	6	6	15.18	14.84
50kV, 150 Pulses	4.22	4.28	0.19	0.19	6	6	15.18	14.56
50kV,300 Pulses	4.21	4.26	0.19	0.18	6	6	15.12	14.56
50Kv, 300 Pulses (–ve)	4.22	4.25	0.19	0.18	6	6	15.12	14.56

Table. 4 : Microbial test result for continuous process.

SAMPLE	MICROBIAL COUNT		% GROWTH
	1ST DAY	7TH DAY	
Control Sample	6940	9680	28
30kV, 150 Pulses	1050	1300	19
50kV, 150 Pulses	560	670	16
50kV,300 Pulses	340	380	11
50Kv, 300 Pulses (– ve impulse)	330	370	11

From the above table, it is analyzed that effective microbial reduction can be achieved by applying PEF without affecting its chemical and nutritional properties.

The comparison of microbiological test for the fruit juice samples treated by static process and continuous process has been listed below. Table 5 gives the comparision for tomato juice preservation with static and continuous process.

Table 3 comparison of results

SAMPLE	% Growth of microbiological content	
	STATIC CHAMBER	CONTINUOUS CHAMBER
Control Sample	32	28
30kV, 150 Pulses	28	19
50kV, 150Pulses	24	16
50kV, 300 Pulses	18	11
50kV, 300 (-ve) Pulses	16	11

Table 4 gives the comparision for tomato juice preservation.

From the above table it can be seen that shelf life extension can be achieved by continuous process treatment method as like that of static process.

IV. CONCLUSION

In this work various PEF treatment chambers were studied, and the co-axial continuous flow treatment chamber design is fabricated for PEF treatment of tomato juice. From the above result it can be seen that shelf life extension of the tomato juice has been achieved in continuous process as like that of static process. Contrary to static process, liquid food can be treated continuously and thus it can be used to treat huge quantity of liquid food in commercial scale.

ACKNOWLEDGEMENT

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Entity Relationship Modelling of Jewellery Mall Applying Object Disclosure Strategy

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Abstract - In this paper, we will be designing a simple shopping mall using object oriented technology. The mall will provide a soothing shopping experience for customers, while at the same time allowing us to explore design patterns and other features object oriented technology. Shopping malls contribute to business more significantly than traditional markets which were viewed as simple convergence of supply and demand. Shopping malls attract buyers and sellers, and induce customers providing enough time to make choices as well as a recreational means of shopping. This study examines the activities of some of three different shops and their quality working given to the people

Keywords - *Shopping mall sector , Unified Framework, entertainment, purchase, Unified Modeling Language, semantics.*

I. INTRODUCTION

Software is very abstract and hard to visualise. A visual modelling language, such as UML, allows software to be visualised in multiple dimension, so that a computer system can be completely designed before construction work starts. Furthermore, UML can be used to produce several models at increasing levels of detail.

The overall plan of the software can quickly and easily be defined at the start of the project with a high level model allowing for accurate estimation. Increasing levels of detail can then be added to each part of the software as it is constructed, until finally the software is developed.

UML is applicable for both new developed and already existing systems. It is been wrongly understanded that a older system should be Re-documented for the application of newer application into it. It also improves the quality of the software engineering staffs as most of the engineers look for the company modeled with UML. The Unified Modelling Language was created by Rational Software in order to provide a standard for software modelling languages an independent organisation.

UML is a universal language because it can be applied in many areas of software development. It includes user-defined extensions so that it can be adapted for specific environments. Industrial standard extensions now available for business modelling and web-based applications development.

The Use Case Gives the nature of modelling with UML ensuring that all levels of model trace back resembles elements of the original functional requirements. This traceability between models comes without the extra effort of creating and maintaining a 'traceability matrix' which can be a complex and time consuming job.

As a result of this the required changes for the document can easily be made. With the help of this UML any requirement changes can be made without any intreruption to other requirements even the lines. If any changes were been effected then that can be easily been changed without any difficulties. In many design processes, the use case diagram is the first that designers will work with when starting a project. This diagram allows for the specification of high level user goals that the system must carry out. These goals are not necessarily tasks or actions, but can be more general required functionality of the system.

II. USE CASE DIAGRAM

UML Use Case Diagrams can be used to describe the functionality of a system in a horizontal way. That is rather than representing the details of individual features of an system. UCDs can be used to show all of its available functionality. It is should be noted that a USD

is different from the flow chart, sequence diagrams because these diagrams won't explain the details about the next execution and sub-execution steps of the system.

The UCD have 4 major elements, the use case diagram depicit:

- **Use cases -** A use case describes a sequence of actions that provide something of measurable value to an actor and it is drawn as a horizontal ellipse.
- **Actors -** An actor is a person, organization, or external system that plays a role in one or more interactions with your system. Actors are drawn as stick figures.
- **Associations** - Associations between actors and use cases are indicated in use case diagrams by solid lines. An association exists whenever an actor is involved with an interaction described by a use case. Associations are modeled as lines connecting use cases and actors to one another, with an optional arrowhead on one end of the line. The arrowhead is often used to indicating the direction of the initial invocation of the relationship or to indicate the primary actor within the use case. The arrowheads are typically confused with data flow and as a result I avoid their use.
- **System boundary boxes (optional)** - You can draw a rectangle around the use cases, called the system boundary box, to indicates the scope of your system. Anything within the box represents functionality that is in scope and anything outside the box is not. System boundary boxes are rarely used, although on occasion I have used them to identify which use cases will be delivered in each major release of a system.
- **Packages (optional)** - Packages are UML constructs that enable you to organize model elements (such as use cases) into groups. Packages are depicted as file folders and can be used on any of the UML diagrams, including both use case diagrams and class diagrams. I use packages only when my diagrams become unwieldy, which generally implies they cannot be printed on a single Page.

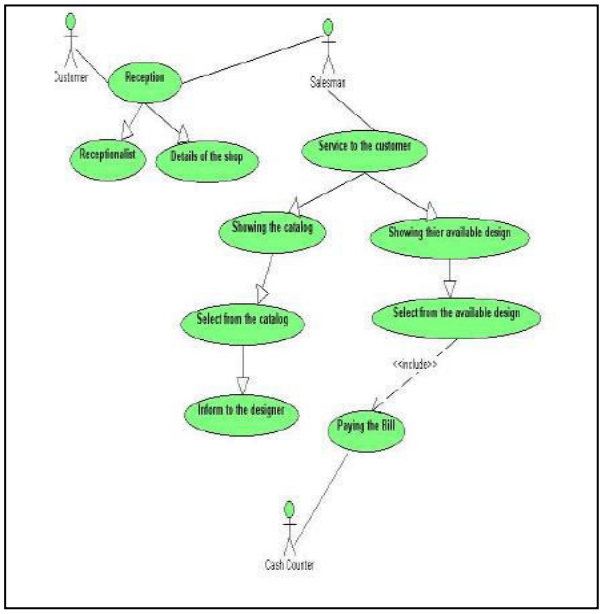

Fig. 1 : User case diagram for Jewellery Shop

The above use case diagram gives the overview of the jewellery shop. When a customer goes to a jewellery shop, he would be asked the details to the receptionist in the shop. The receptionist gives the details about the shop and inform to the salesman. The salesman service to the customer and he will show the available design else he will show the catalog. Suppose the customer select from the catalog, the salesman inform to the designer about the designe, otherwise the customer will select from the available design and he should be paying the bill in the cash counter.

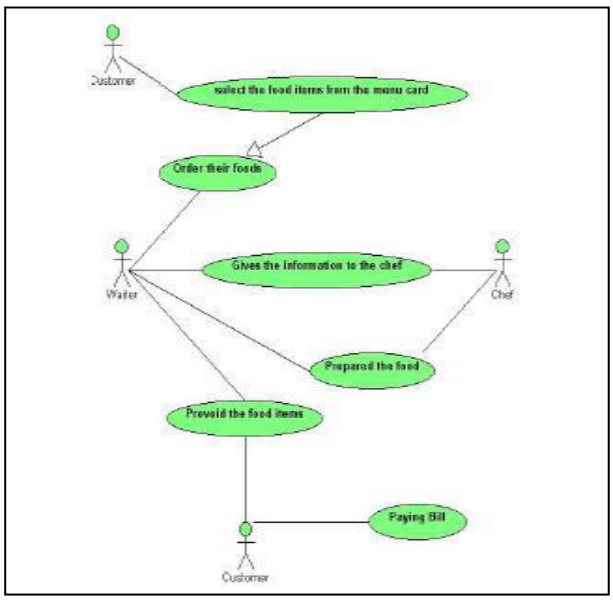

Fig. 2 : Use case diagram for Restaurant

The above use case diagram gives the process in the restaurant. When a customer goes to the restaurant, he would be selecting the food items from the 'menu card' and order their food items to the waiter. The waiter informs to the chef of the restaurant. The chef will make the food and gives to the waiter and the waiter will be serving to the customer. The customer after having their food pays the bill to the cashier.

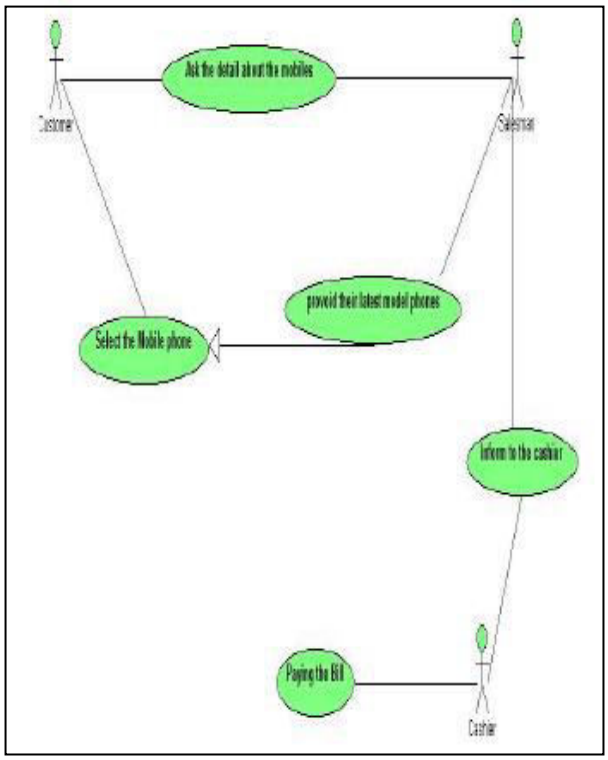

Fig. 3 : Use case diagram Mobile Shop

The above use case diagram gives the details in the mobile shop. When a customer goes to a mobile shop, he would ask the details about the latest model mobile phones to the salesman in the mobile shop. The salesman provides the details to the customer, so as he can select his required model of mobile phone. The salesman asks the details of the customers such as his/her name, address, phone number, id proof etc, and inform it to the cashier. The cashier will make the bill and gives to the customer. The customer pays the bill.

III. INTERACTION DIAGRAM

Interaction diagrams are models that describe how a group of objects collaborate in some behavior - typically a single use-case. The diagrams show a number of example objects and the messages that are passed between these objects within the use-case.

Interaction diagrams should be used when you want to look at the behavior of several objects within a single use case. They are good at showing the collaborations between the objects, they are not so good at precise definition of the behavior. If we want to look at the behavior of a single object across many use-cases then use of State Transition Diagram. If you want to look at behavior of many use cases or many threads, consider an activity diagram. Much like the class diagram, developers typically think sequence diagrams were meant exclusively for them. However, an organization's business staff can find sequence diagrams useful to communicate how the business currently works by showing how various business objects interact. During the requirements phase of a project, analysts can take use cases to the next level by providing a more formal level of refinement. When that occurs, use cases are often refined into one or more sequence diagrams.

- **Purpose**

The main purpose of a sequence diagram is to define event sequences that result in some desired outcome. The diagram conveys this information along the horizontal and vertical dimensions: the vertical dimension shows, top down, the time sequence of messages/calls as they occur, and the horizontal dimension shows, left to right, the object instances that the messages are sent to.

- **Lifelines**

When drawing a sequence diagram, lifeline notation elements are placed across the top of the diagram. Lifelines represent either roles or object instances that participate in the sequence being modeled. In fully modeled systems the objects (instances of classes) will also be modeled on a system's class diagram.

Lifelines are drawn as a box with a dashed line descending from Messages.

- **Messages**

The first message of a sequence diagram always starts at the top and is typically located on the left side of the diagram for readability. Subsequent messages are then added to the diagram slightly lower than the previous message. At the center of the bottom edge the lifeline's name is placed inside the box.

- **Guards**

When modeling object interactions, there will be times when a condition must be met for a message to be sent to the object. Guards are used throughout UML diagrams to control flow. Here, I will discuss guards in both UML 1.x as well as UML 2.0. In UML 1.x, a guard could only be assigned to a single message. To draw a guard on a sequence diagram in UML 1.x, you placed the guard element above the message line being guarded and in front of the message name.

Except for the activity nodes the other notation elements of interaction overview diagrams are the same as for activity diagrams, such as initial, final, decision, merge, fork and join nodes. The two new elements in the interaction overview diagrams are the "interaction occurrences" and "interaction element. UML 2 has introduced significant improvements to the capabilities of sequence diagrams. Most of these improvements are based on the idea of interaction fragments which represent smaller pieces of an enclosing interaction. Multiple interaction fragments are combined to create a variety of combined fragments, which are then used to model interactions that include parallelism, conditional branches, optional interactions.

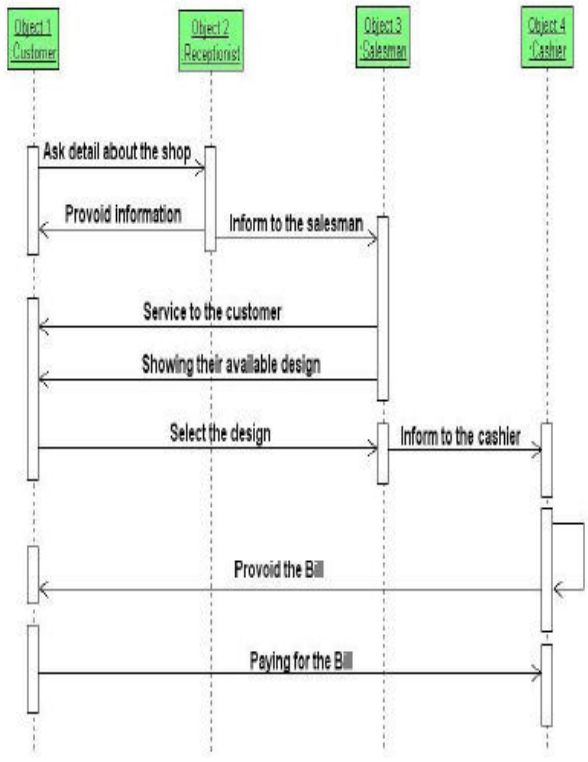

Fig. 4 : Sequence diagram for Jewellery Shop

The customer in order to buy a jewels he/she asks the information about the shop to the receptionist. Receptionist gives the necessary details to the customer and inform the arrival of customer to the salesman, so he can service the customer. Salesman shows the available designs in their shop to the customer. After the selection of model(s) by the customer it will be informed to the salesman. Salesman informs about the details and design of the selected model to the cashier. Cashier provides the bill to the customer and the customers pays for it.

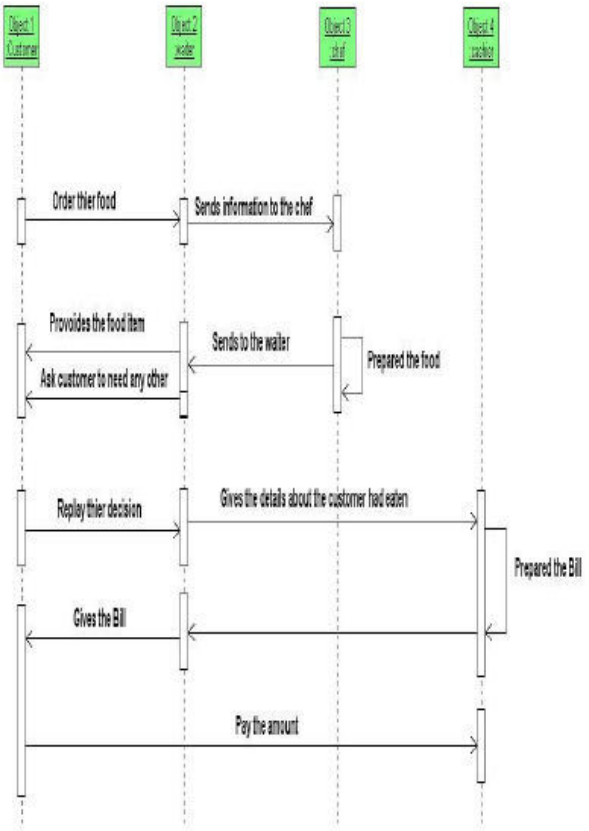

Fig. 5 : Sequence diagram for Restaurant

The customers after entering into the restaurant order their foods from the menu card to the waiter of the restaurant. Waiter informs about the food items to the chef, on receiving the information from the waiter chef prepares the food items as per the need and gives them to the waiter. Waiter serves the f ood to the customer, and asks for other needs. After geting the response of the customer waiter informs about the food items to the cashier. Cashier prepares the bill and give it to the waiter. Waiter provides customer the bill, the customers pays the bill amount to the cashier.

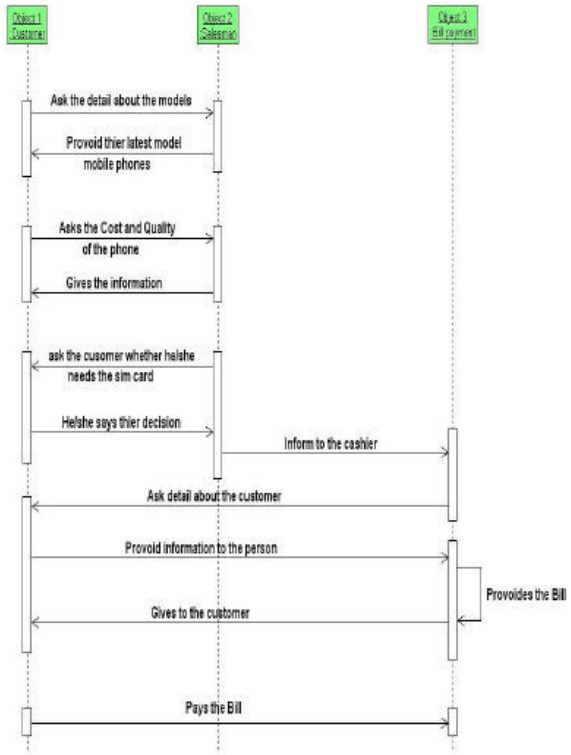

Fig. 6 : Sequence diagram for Mobile shop

The customer enters into the mobile shop and asks the details of the available models to the salesman. Salesman provides the latest models of mobile phones to the customer. After selecting several models, customer asks the quality and cost of each models. salesman gives all the needed information to the customer. After the selection of an model by the customer salesman asks the customer whether he/she needs the sim card . After asking the decision of the customer salesman informs the to the cashier. Cashier asks the details of the customer he/she provides the needed information to the cashier. After getting the information cashier prepares and provides the bill to the customer. Customer pays the bill amount.

IV. ACTIVITY DIAGRAM

UML 2 activity diagrams are typically used for business process modeling, for modeling the logic captured by a single use case or usage scenario, or for modeling the detailed logic of a business rule. Although UML activity diagrams could potentially model the internal logic of a complex operation it would be far better to simply rewrite the operation so that it is simple enough that you don't require an activity diagram. In many ways UML activity diagrams are the object-oriented equivalent of flow charts and data flow diagrams (DFDs) from structured development.

- **Initial node** - The filled circle is the starting point required even it can make it significantly easier to read the diagram.
- **Activity final node -** The filled circle with a border is the ending point. An activity diagram can have no or many activity final nodes.
- **Activity** - The rounded rectangles represent activities that occur. An activity may be physical, such as Inspect Forms, or electronic, such as Display Create Student Screen.
- **Flow/edge** - The arrows on the diagram. Although there is a subtle difference between flows and edges I have never seen a practical purpose for the difference although I have no doubt one exists. I'll use the term flow.
- **Fork** - A black bar with one flow going into it and several leaving it. This denotes the beginning of parallel activity.
- **Join** - A black bar with several flows entering it and one leaving it. All flows going into the join must reach it before processing may continue. This denotes the end of parallel processing.
- **Condition** - Text such as [Incorrect Form] on a flow, defining a guard which must evaluate to true in order to traverse the node.
- **Decision** - A diamond with one flow entering and several leaving. The flows leaving include conditions although some modelers will not indicate the conditions if it is obvious.
- **Merge** - A diamond with several flows entering and one leaving. The implication is that one or more incoming flows must reach this point until processing continues, based on any guards on the outgoing flow.
- **Partition** - It also called swimlanes, indicating who/what is performing the activities (either the Applicant, Registrar, or System).
- **Sub-activity indicator -** The rake in the bottom corner of an activity, such as in the Apply to University activity, indicates that the activity is described by a more finely detailed activity diagram.
- **Flow final -** The circle with the X through it. This indicates that the process stops at this point.

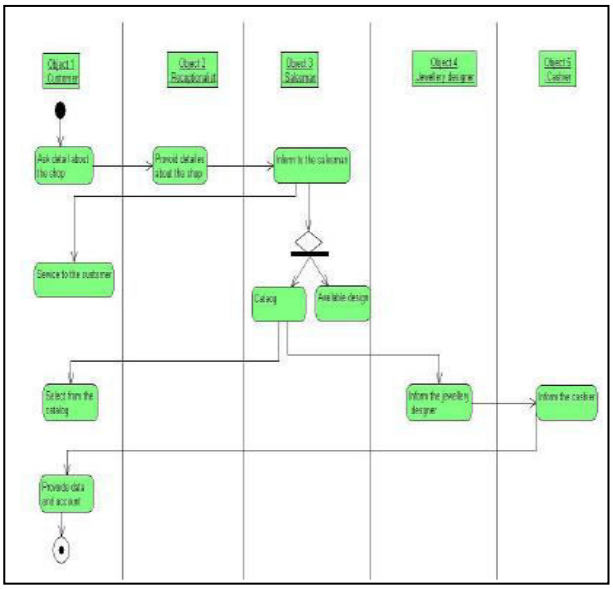

Fig.7 : Activity Diagram for a Jewellery Shop

The customer enter into the shop and asks for the information about the shop to the receptionist. So she provides the necessary information and send them to a salesman. Salesman serves them by showing all the available models in their shop and as per the customer need through jewels or by catalogs, so as to it is easily been selected by the customers. If the model is being selected from the catalog it is been informed to the jewellery designer about the designs. After the information delivery the salesman inform about it to the cashier. Cashier prepares the bill for the customer and provide them. Customers pays the bill for thier respective models.

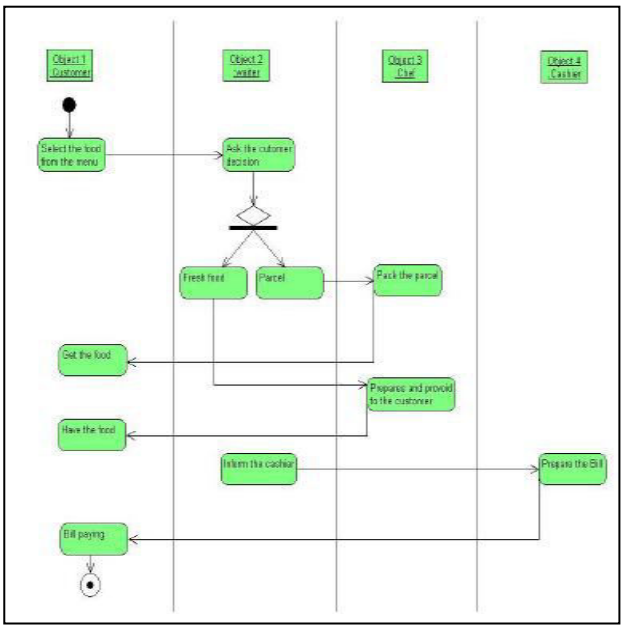

Fig. 8 : Activity Diagram for a Restaurant

Once the customer had been entered into the shop he can select the food as per his needs from the menu card and inform about it to the waiter . Waiter delivers the information to the chef of that restaurant . Chef on getting the information of types of foods he prepares the food to the customer and deliver them to the waiter . Waiter serves the food to the customers and asks for their further needs of food . After getting their decisions he inform about the food items to the cashier. Cashier prepares the bill and give it to the waiter. Waiter provides it to the customer. Customer pays the bill to the cashier.

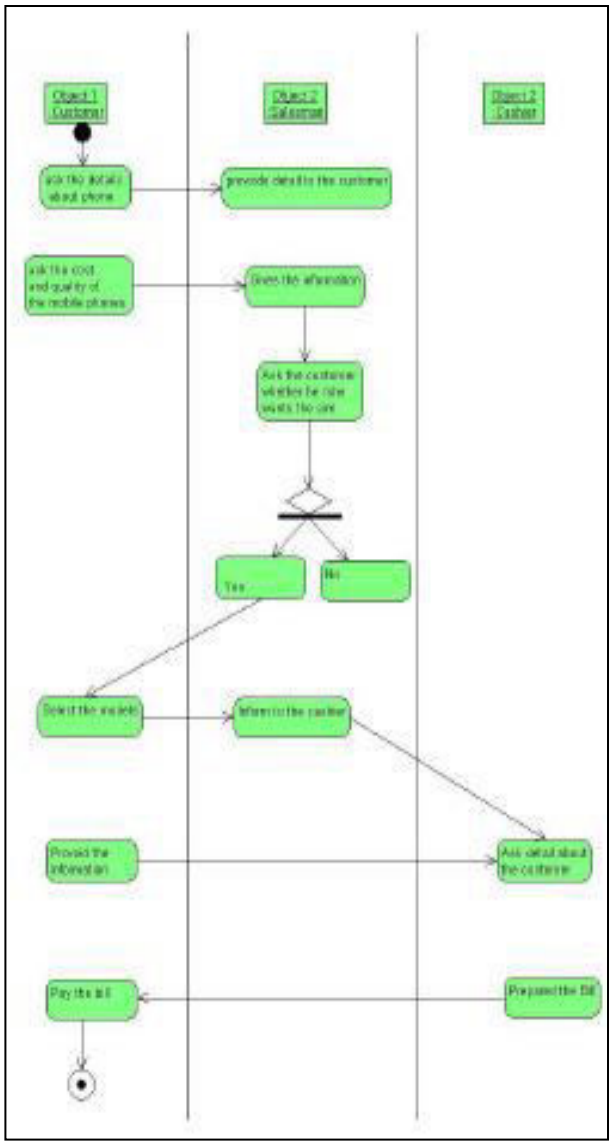

Fig. 9 : Activity Diagram for a Mobile Phone

Customer enters into the mobile shop and asks for the latest models of available mobile phones. Salesman now gives the necessary details and shows the customer for the available models in their shop. Customer selects

some models among the showned models and asks for the information about the required models and select a model. Salesman enquires the customer whether they need a sim card. After getting the decision he informs about that to the cashier. Cashier gets the information about the customer and prepares the bill for the respective mobile model and provide it to the customer, customer pays the amount for the bill and gets his product.

V. CONCLUSION AND FUTURE WORK

After the analysis of the above data we came to a conclusion that most of the people prefer malls for purchasing branded products because it provides them all under an single roof. People generally buy clothes and food items from malls. People prefer shopping in neighborhood stores because of cast selection & choice, presence of various alternative shops and reasonable price. People are more safe and comfortable while shopping in malls. People are quit satisfied with the facilities provided by malls.

Above we have discussed about the various use case diagrams, interaction diagrams, activity diagrams of various shops belonging to an shopping mall. This way path helps us to visualize the entities and the relationship between those entities and also let us to visualize the feature E-R diagram. The same paper can be expanded using the Java Eclipse as an front end and ASP.NET as an back end. By taking this as an initial step we are proceeding over the work to incorporate the current technologies.

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Applying Object Oriented Strategy to Model an Educational Administration Structure for Secured Databases

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Abstract - Recent years have observed a steep rise in substantial financial resources spent against education sector. Ensuring a high operational efficiency in the sector turns out to be the most essential goal for evaluating the organizational performance as a whole. This work aims to employ a modeling language aimed to provide a unified framework for representing an effective and efficient college management system, which implicitly ensures the privacy and confidentiality of the information and messages. The proposed modeling methodology is based on the principle of object orientation, which allows describing both software and functionalities explicitly. Furthermore, it is illustrated how the well-known object-oriented specification language unified modeling language can be adopted, to provided an adequate formalization of its semantics, to describe structural and behavioral aspects of college database management system related to both logical and physical parts. It is needed to implement the software on the basis of Object Oriented Model developed. Flaw in modeling process can substantially contribute to the development cost and time. The operational efficiency may be affected as well. Therefore special attention should be paid to the correctness of the models that are used at all planning levels and hence Unified Modeling Language (UML) takes its impeccable role.

Keywords - *college management, Unified Framework, Privacy, Confidentiality, Unified Modeling Language, Semantics.*

I. INTRODUCTION

UML or Unified Modelling Language is a specification language which is used in the software engineering field .It is the general purpose language that uses a graphical designation that is used to create an abstract model. This model is used in the system. This system is called the UML model. This object management group is responsible for defining UML and they perform this via UML meta model.

The UML is commonly used for visualizing and computing software intensive. It is due to software complexity in recent years, the developers are facing more complexity to build a complex applications in a short period of time. Even though when the developers do they are often filled with bugs, it may take the programmers weeks to find and fix them. In this time has been wasted since an approach could have been used which would have reduced the number of error before the application was completed. However it should be emphasized that UML is not simply used for modeling the software it can be also used to create models for the system engineering ,business organization. A special language called System Modelling Language which has been designed in order to handle the system that are defined withinUML2.0.The Unified Modeling language is important due to many reasons .First is that it has been used is the catalyst in the advanced technology which are model driven and some of these includes the modern driven development. UML 2.0 defines thirteen types of diagrams, divided into three categories: Six diagram types represent static application structure; three represent general types of behavior; and four represent different aspects of interactions:

Structure Diagrams include the Class Diagram, Object Diagram, Component Diagram, Composite Structure Diagram, Package Diagram, and Deployment Diagram.

Behavior Diagrams include the Use Case Diagram (used by some methodologies during requirements gathering); Activity Diagram, and State Machine Diagram.

Interaction Diagrams, all derived from the more general Behavior Diagram, include the Sequence Diagram, Communication Diagram, Timing Diagram, and Interaction Overview Diagram.

II. CLASS DIAGRAM

Class diagram models the static structure of the system using objects, attributes, operations and relationships. Applying Object Oriented Strategy to Model an Educational Administration Structure for Secured Databases

The relationship between various attributes can be clearly described using the various symbols.

- Objects : The objects are the entities that shares the attributes of the class. The objects can be a real world entity. For example let us consider the library management system in which each person who borrows book from a library in considered as an object of the class user. The objects shares the attributes and operations of the class. In general an object is a medium through which we can access the class attributes

- Attributes & Operations : The attributes are the variables that holds the value for an object. It may of any data type but the user need to specify the data type while declaring a class. The attributes are also called as the "data members". The operations denotes the actions or the functions that are performed by an object. An operation is also called as a "member function",

- Relationships: The relationship describes the relation between various classes or objects in an class diagram. The relationship denotes the mode of communication that exists between the classes. There are various types of relations that occurs between classes in an class diagram and they are described below

1. Containment: It denotes that the two classes are strongly connected. For example consider the relation between the internet and search engines there exists a strong relation between these two classes (i.e) without search engines we cannot access the internet. This relation is being denoted by a shaded diamond pointer.

2. Aggregation: It denotes the weak relation that exists between two or more classes. This relation shows that a particular class may or may not be present in the modeling process. It is denoted by a hollow diamond pointer.

3. Association : It denotes the associated relationship that exists between two classes. It is denoted by an straight line.

4. Inheritance : This relation describes the inheritance relation that exists between two classes. The inheritance is an important feature of a object oriented data model. It helps in the reusability of the codes. The inheritance helps in inheriting the attributes and member functions of the parent class to the child class. It is denoted by an hollow triangle pointer.

5. Cardinality : It describes the number of occurrences happening in an event. Normally it specifies how the occurrence of an object is connected to the occurrence of another object. The cardinality relation can be of many types such as one-one relation, one-many relation, many-one relation and many-many relation. It is denoted by specifying the type of cardinality above the arrow headed line.

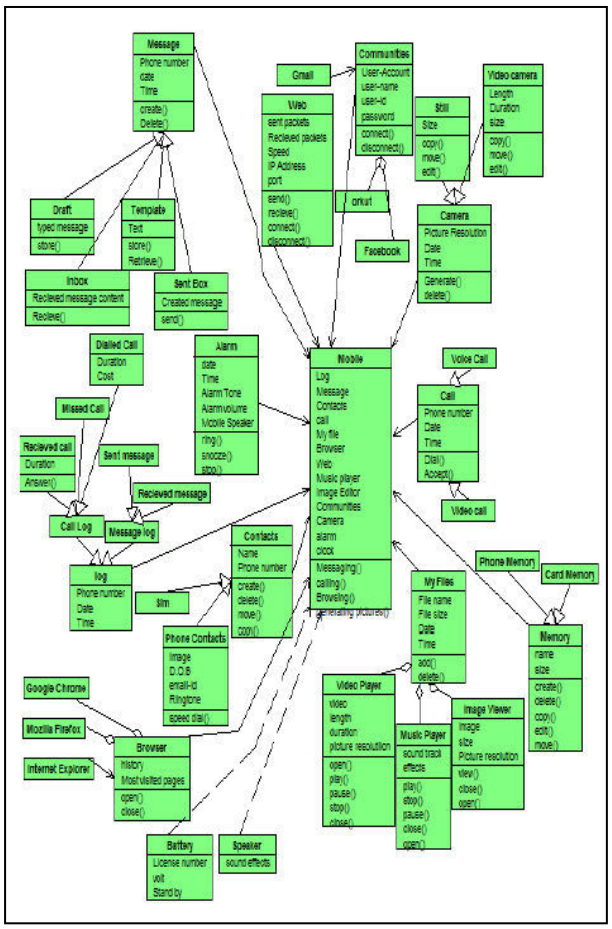


Fig. 1 : Class Diagram for College Management System

The above class diagram shows the various classes and the relation that exists between those classes in an college management system. Here college is the important class that controls the activities and operations of the various objects of other classes. The college management system consists various classes such as hostel, student, faculty, department, library, etc. The

class hostel is inherited into boys_hostel and girls_hostel so that both the classes can share the same data members and member functions. Similarly the class faculty is inherited into teaching and non-teaching staff. Further the class non-teaching staff is divided into employees including securities, office workers and lab assistants. All these can be extended as they have inheritance relation.

III. USE CASE DIAGRAM

A use case describes a sequence of actions that provide something of measurable value to an actor and is drawn as a horizontal ellipse.

Use case diagrams depict:

- Use cases : A use case describes a sequence of actions that provide something of measurable value to an actor and is drawn as a horizontal ellipse.
- Actors : An actor is a person, organization, or external system that plays a role in one or more interactions with your system. Actors are drawn as stick figures.
- Associations : Associations between actors and use cases are indicated in use case diagrams by solid lines. An association exists whenever an actor is involved with an interaction described by a use case. Associations are modeled as lines connecting use cases and actors to one another, with an optional arrowhead on one end of the line. The arrowhead is often used to indicating the direction of the initial invocation of the relationship or to indicate the primary actor within the use case. The arrowheads are typically confused with data flow and as a result I avoid their use.
- System boundary boxes : The rectangular box which is drawn around the use case is known as system boundary boxes, which is used to indicate the scope of our system Anything within the box represents functionality that is in scope and anything outside the box is not. System boundary boxes are rarely used, although on occasion I have used them to identify which use cases will be delivered in each major release of a system
- Packages : Packages are UML constructs that enable you to organize model elements (such as use cases) into groups. Packages are depicted as file folders and can be used on any of the UML diagrams, including both use case diagrams and class diagrams. I use packages only when my diagrams become unwieldy, which generally implies they cannot be printed on a single page, to organize a large diagram into smaller ones.

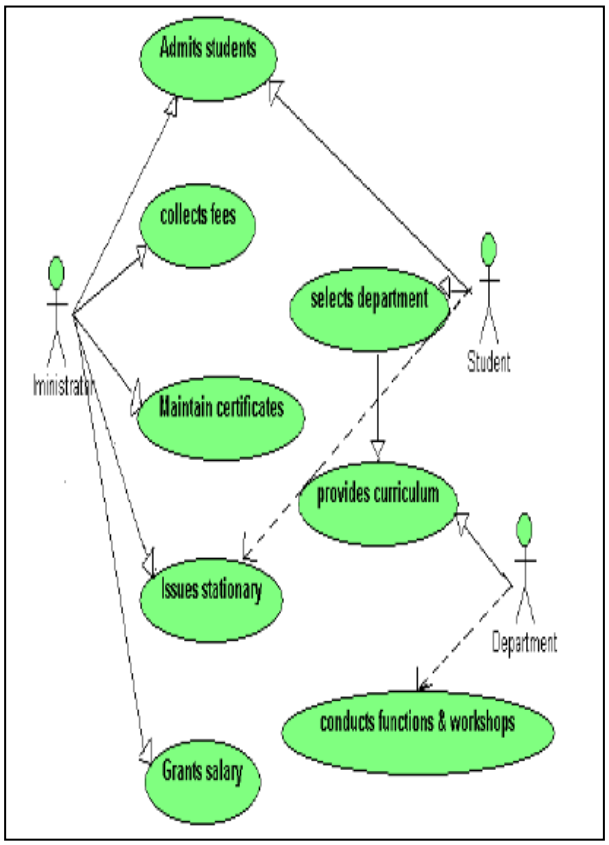


Fig. 2 : User case diagram for student admission

The above use case diagram gives the overview of college management system for the admission of a student into the institution. Here the administrator haves the capability to admit a student after checking for his eligibility(i.e)if he is qualified. From a student side he will consult the administrator for the facilities available in that institution once he meets his needs he will surely join in tat college. After a student is admitted in the college he have to pay his fees in order to confirm his seat. All the students should submit their original certificates including their marksheets, community certificate, etc.These certificates are being maintained in the administration by the administrator during the course period. In case of department the students have their rights to choose a particular department which they would like to choose. The work of a department is to provide curriculum for the students and they also organize many functions, seminars and workshops. The administrator issues the stationary items to the students and once a student receives it then money will be actually debited from his account.

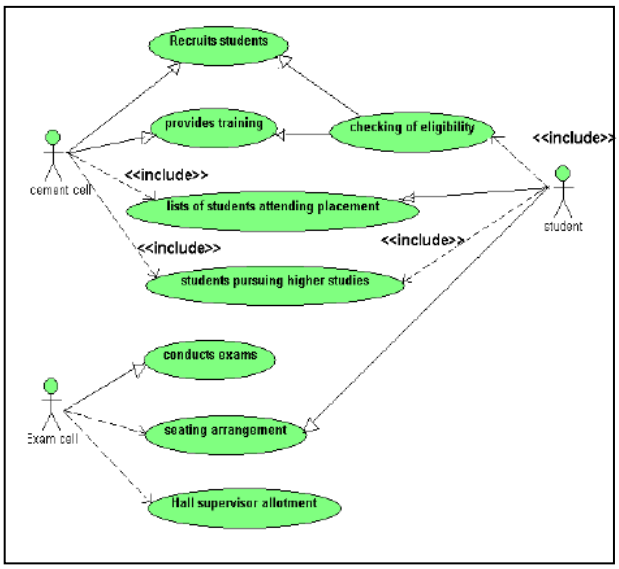


Fig. 3 : Use case diagram for attending placement & exams

The above use case diagram shows the actions performed by a student in attending placements and exams. First let us consider the actions that are being performed by the placement cell. The main duty of a placement cell is to provide training to the students so that the students can face their placement with high level of confidence. It also provides the job opportunities for the students in various leading concerns. For a student to undergo placement he should satisfy the necessary conditions that are being proposed by the placement coordinator. This placement cell also contains information about the number of students attending placements in addition it also contains information about the students who are going to pursue their higher studies. Next we consider the actions that are being performed by the exam cell. The exam cell is responsible for scheduling the exams according to the department and year of course.

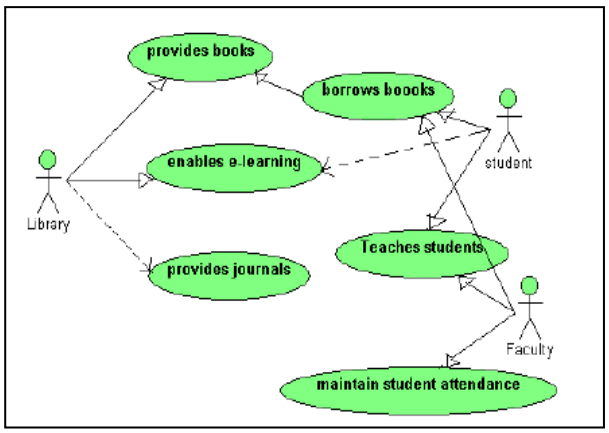


Fig. 4 : Use case diagram for relation between student, library & faculty

The above use case diagram shows the relation between a student, library and faculty. Both the students and the faculty members borrows books from library. The library also enables e-learning facility so that both the student and faculty can gain extra knowledge about the current trends. This also helps the students in getting more information in their area of interest.

IV. INTERACTION DIAGRAM

Interaction diagrams are used to model the behaviour of the use cases by describing the way in which the group of objects interact to the complete task. There are two types of interaction diagram sequence and calibration diagram. In order to model the behaviour of the several objects in a use case diagram interaction diagrams are used. This diagram is to demonstrate how the object supports for the behavior. Meanwhile the collaboration diagram does not give the deep representation of the behaviour. The interaction of object in the use case is done by sequence diagram, collaboration diagram or by both diagrams. The sequence diagrams are used to represent the sequence of events that occurs collaboration diagrams are used to represent how the objects are connected.

The interactions which has occurred are shown by the sequence diagram in the sequential order.

Diagram Elements:

- **Object -** Each of the objects that participate in the sequence diagram. It is drawn across the top. Note that objects are used in this diagram while classes are used in use cases, class diagrams.
- **Lifeline -** A dotted line is dropped from each object in the sequence diagram. Arrows terminating on the lifeline indicate messages (commands) sent to the object. Arrows originating on the lifeline indicate messages sent from this object to another object. Time flows from top to bottom on a sequence diagram.
- **Active -** To indicate that an object is executing, i.e., it has control of the CPU, the lifeline is drawn as a thin rectangle.
- **Message -** A horizontal arrow represents a message (command) sent from one object to another. Note that parameters can be passed as part of the message and can (optionally) be noted on the diagram.
- **Return -** When one object commands another, a value is often returned. This may be a value

computed by the object as a result of the command or a return code indicating whether the object completed processing the command successfully. In some instances the object may not be able to return this information immediately. This indicates the flow of information was based on a previous request.

- **Iteration -** Square brackets preceeded by an asterisk (*) indicate iteration. The message is sent multiple times. The expression within the brackets describes the iteration rule.

- **Deletion -** An X is used to indicate the termination (deletion) of an object.

The below diagram shows the sequence of operations that are being performed whan a student approaches the college administration for admission. Once if a particular student is admitted he has to pay fees to conform his admission. Then the administration also appoints the staffs for each departments according to their qualification.

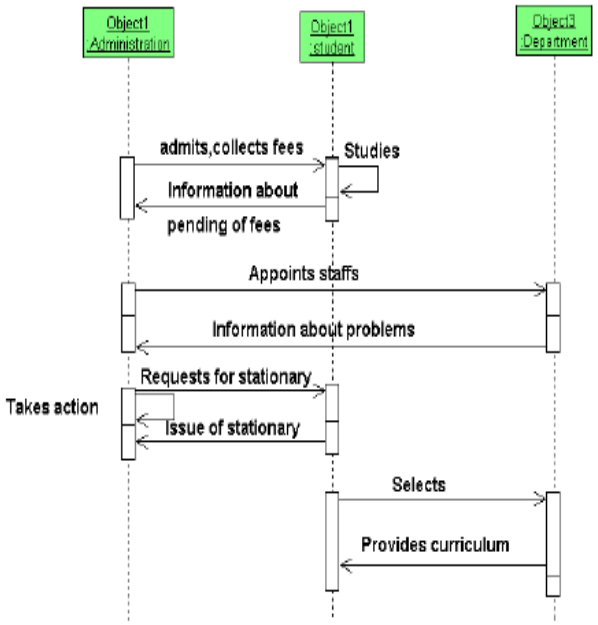


Fig. 5 : Sequence diagram for student admission

The below diagram shows the series of operations that are being performed while conducting placement and exams for the students. The students are first trained irrespective of any qualification but they are allowed to attend placements based on their cgpa, discipline and so on. Such conditions are being checked. The exam cell schedules all the exams it also allots hall supervisors, seating arrangement for students.

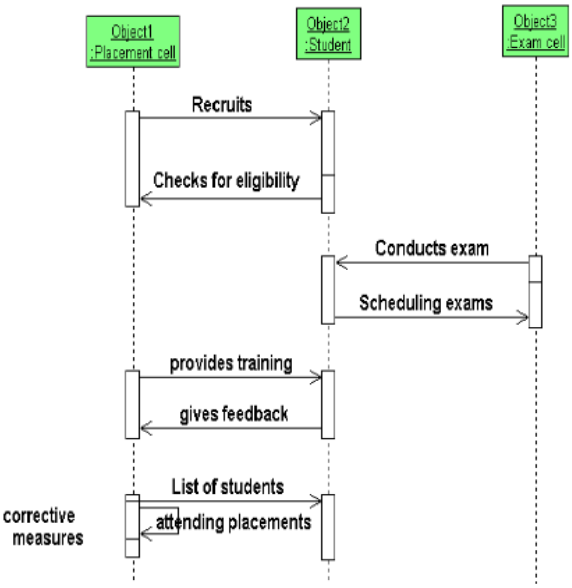


Fig. 6 : Sequence diagram for conducting placement & exams

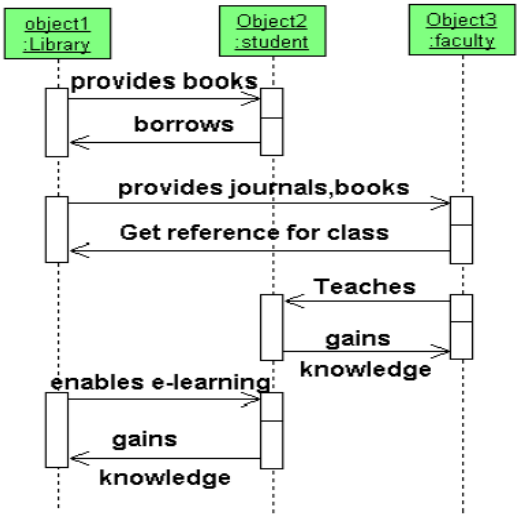


Fig. 7 : Sequence diagram for borrowing books from library

The above sequence diagram shows the sequence of steps involved in borrowing a book from library. Both the students and faculty can borrow books from library. The books are issued only after entering the details into the library database. The students or faculty are not allowed to take books if they are not authenticated

V. ACTIVITY DIAGRAM

An activity diagram emphasizes on the dynamic behaviour of the system by showing collaboration among object changes to the internal states of object.

The activity diagram is the dynamic structural view of a problem.

- Initial Node

  An initial or start node is depicted by a large black spot.

- Final Node

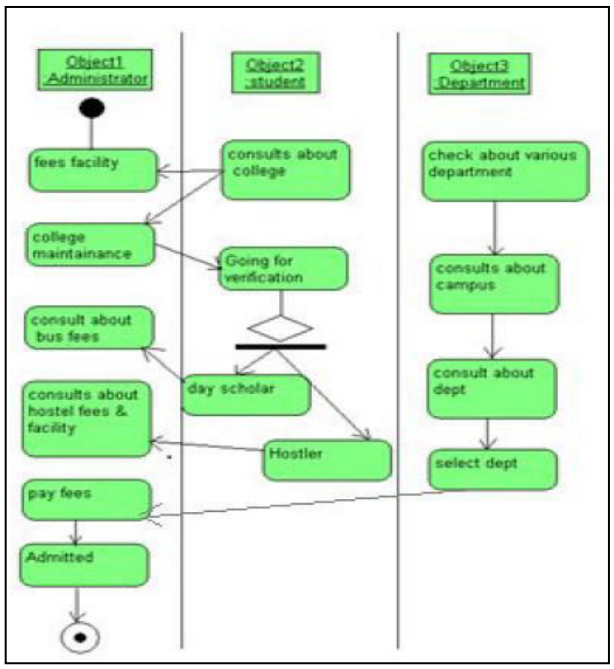
In activity diagrams there are two types of final nodes activity and flow final node .The flow final node is indicated as circle with the cross inside the activity final node denotes end of all the control flows in the activity.

- Fork and join nodes:

Forks and joins have the same notations. They are either represented either by vertical or horizontal bar. These are used to indicate the starts and ends of the threads.

- Decision and Merge Nodes:

Decision nodes and merge nodes have the same notation: a diamond shape. These both be named. The control flows coming away from a decision node will have guard conditions which will allow control to flow if the guard condition is met.



When a student goes to a college for admission he consults the administration office for fees details and infrastructure. Before getting admitted he must select the department. Then the students are categorized as day scholars and hostlers. The day scholars collects information about the bus fees and other fees whereas a hostler collects information about the mess fees and hostel fees. At last the student's certificates are verified and the student is admitted.

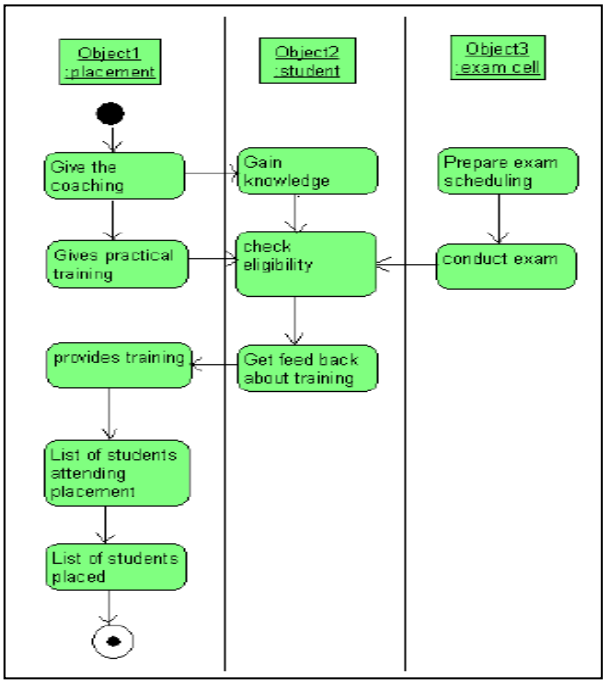


Fig. 8 : Activity diagram for attending placement and exam

The placement sector gives training to all the students and it also receives feedback from the students regarding the training. It contains details about the students academics and also about their extra and co-curicular activities that they perform during their course.

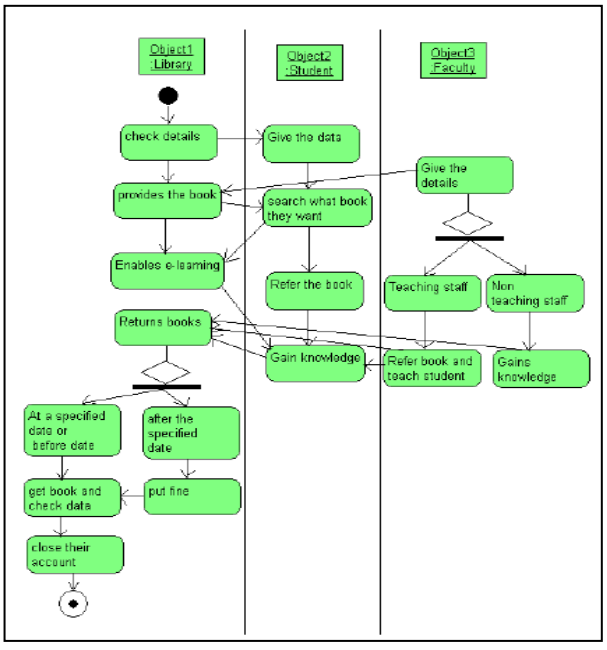


Fig. 9 : Activity diagram for borrowing book from library

The student can borrow book from library while borrowing a book from library the students are assigned to return the book in a specified date. But if the student is failed to return the book at the specified date he/she has to pay fine and then only he can be able to return his book. Once if a student lost or damages the book he have to pay penalty. The library also provides earning facility with which the user can be able to access books through internet. They can also use internet to study various standard papers that are being published by the research scholars.

VI. CONCLUSION AND FUTURE WORK

The paper has focused on the essential and extended Object Oriented features of a College Management System. Various models of UML have been employed to analyze the static, dynamic and functional view of the system. In spite of several user-friendly, time-saving, more efficient, convenient and flexible options provided by banks in the virtual space, College Management System has not achieved a major break-through that it deserves. However if an Object Oriented approach is adopted while building the software, an explosive growth in College Management System arena could be traced. Paper could be implemented using VB.net as front end and any reliable database system such as Oracle, as back end, and testing could be carried out by Rational Test Manager. The paper depicts the structural and behavioral aspects of online personal finance management system related to both logical and physical parts. It is a fact that design flaws that surface during implementation are most costly to fix than those that are found earlier. Focusing on implementation issues too early restricts the design choices and often leads to inferior product. Hence the developed object-oriented approach encourages software developers to work and think in terms of application domain through most of the software engineering lifecycle. Since flaw in modeling process can substantially contribute to the development cost and time and affect the operational efficiency special attention is paid to the correctness of the UML models that are used at all planning levels rather than focusing much on implementation issues.

ACKNOWLEDGEMENT

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SISO-WPMCM and SISO-OFDM Channel Estimation using Pilot Carriers

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Abstract - As proven by the success of OFDM, multicarrier modulation has been recognized as an efficient solution for wireless communications. Waveform bases other than sine functions could similarly be used for multicarrier systems in order to provide an alternative to OFDM. Wavelet Packet based Multi-Carrier Modulation (WPMCM) offers an alternative to OFDM as it has strong advantage of being a generic transmission scheme whose actual characteristics can be widely customized to fulfill several requirements and constraints of an advanced communication systems. This paper addresses channel estimation based on time-domain channel statistics. Using a general model for a slowly fading channel, the estimation of channel at pilot frequencies with conventional Least Square (LS) and Minimum Mean Square (MMSE) estimation algorithms is carried out in AWGN environment and performance of OFDM and WPMCM are evaluated on the basis of Mean Square Error (MSE). Also a study of WPMCM scheme is conducted, and the performance comparison is made against the traditional OFDM system.

Keywords - *OFDM, Multicarrier Modulation, WPMCM, Least Square, Minimum Mean Square Error, Channel Estimation.*

I. INTRODUCTION

Multicarrier modulation (MCM) is very efficient transmission technique for wireless communication system. It divides the information data into many parallel sub-channels of narrow bandwidth, thus making the system less sensitivity to wide-band impulse noise and fast channel fades. Each sub-channel can be designed to have a bandwidth less than the coherence bandwidth of the channel [10]. It increases wireless capacity without increasing bandwidth. Therefore, it can be assumed that each sub-channel experiences flat fading and the demodulator can be implemented without an equalizer. This technique offers more robust against Inter Symbol Interference (ISI) [1] caused by channel dispersions and multipath interference.

OFDM is a multicarrier modulation technique in which the signal processing is made digitally in the frequency domain by using the – IFFT/FFT blocks. Guard time is added to reduce the effects caused by multipath propagation. WPMCM is a novel multicarrier modulation technique and an alternative to the well established OFDM. In WPMCM signal processing is made digitally in the wavelet domain using – IDWT/DWT blocks. Unlike the Fourier bases which are static sines/cosines, WPMCM uses wavelets which offer flexibility and adaptation that can be tailored to satisfy an engineering demand [4].

Channel estimation is required in wireless communication to counter the effects of channel on the signal. A defining characteristic of the wireless channel are the variations of the channel strength over time and over frequency [11]. The pilot based approach is preferred to estimate the channel and equalize the channel effect to receive the correct signal.

This paper is organized as follows: In Section II, we give a brief review of different Multicarrier Modulation Schemes. In Section III, we discuss different channel estimation techniques like LS and MMSE. In section IV and V presents the simulation results and conclusions respectively.

II. MULTICARRIER MODULATION SCHEMES

A. OFDM

A multicarrier communication system with orthogonal sub-carriers is called Orthogonal Frequency Division Multiplex (OFDM) system. The word "orthogonal" indicates that there is a precise mathematical relationship between the frequencies of the carriers in the system. The basic principle of OFDM is to split a high-data-rate sequence into a number of low-rate sequences that are transmitted simultaneously over a number of subcarriers. Inter-symbol interference (ISI) is eliminated almost completely by introducing a guard interval at the start of each OFDM symbol [6]. In

the guard interval, an OFDM symbol is cyclically extended to avoid Inter-carrier interference (ICI). Thus, a highly frequency selective channel is transformed into a large set of individual flat fading, non-frequency selective, narrowband channels [4].

Compressive OFDM transmission system can be efficiently implemented using IFFT at the transmitter side and FFT at the receiver side. The transmitter and receiver blocks of an OFDM communication system are illustrated in Fig.1.

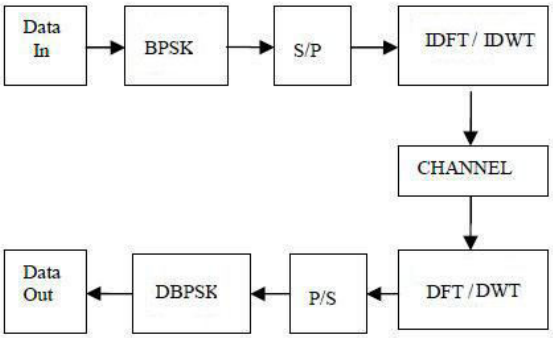

Fig. 1 : OFDM BLOCK

OFDM maximizes spectral efficiency by overlapping subcarrier spectra while maintaining orthogonality between subcarriers. This implies a spacing of unit T_d between each subcarrier frequency.

$$f_k = f_c + k/T_d \quad \text{k=0, 1, 2,..., K-1} \qquad (2.1)$$

Where T_d is the subcarrier symbol duration. A basis of elementary signals to describe the subcarrier symbols is defined as

$$\Psi(n) = g_k(t - nT_d) \quad \text{n= } -\infty \text{ to } +\infty \qquad (2.2)$$

Where,

$$g_k(t) = \begin{cases} e^{j2\pi f_k t}, & 0 \le t \le T_d \\ 0, & t \ge T_d \end{cases} \qquad (2.3)$$

the elementary signals satisfy the orthogonality condition.

B. WPMCM

WPMCM is a multiplexing method that makes use of orthogonal wavelet packets waveforms to combine a collection of parallel signals into a single composite signal. WPMCM systems have overall the same capabilities as OFDM systems with some improved features. One important property of wavelet based transformation is that the waveforms used in general are longer than the transform duration of one symbol [4]. This causes WPMCM symbols to overlap in both time and frequency domain, whereas OFDM overlap only in frequency domain. So, there is no need of guard interval to overcome ISI [3].

In WPMCM system, orthogonality is provided by orthogonal wavelet filters. The real wavelet transform converts real numbers to real numbers, hence the complexity of computation is reduced [1]. Moreover, it's longer basis functions offers higher degree of side lobe suppression and decreases the effects of narrowband interference, ISI, and ICI .

WPMCM employs Inverse Discrete Wavelet Transform (IDWT) at the transmitter side and Discrete Wavelet Transform (DWT) at the receiver side, analogous to the IFFT and FFT used by the OFDM transceivers. In Fig.2 and Fig.3 the IDWT and DWT blocks of a WPMCM communication system are illustrated [2].

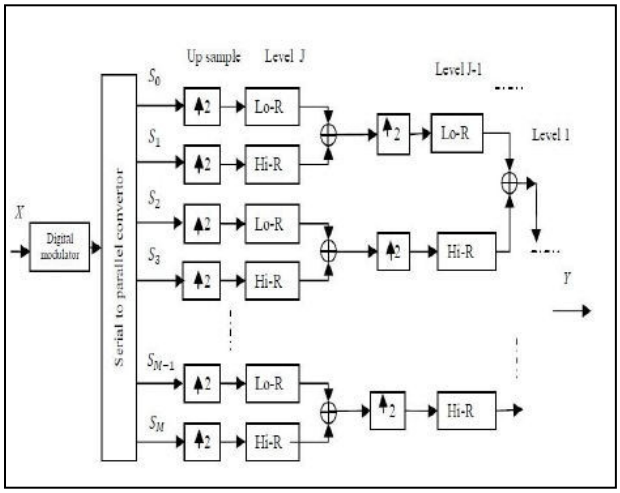

Fig. 2 : IDWT BLOCK

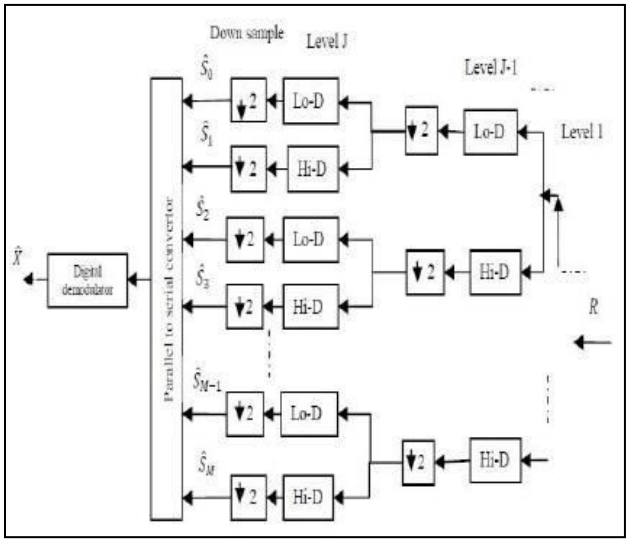

Fig. 3: DWT BLOCK

The WPMCM's waveforms are mutually orthogonal if they satisfy the following condition:

$$\left\langle \xi_l^p(t), \xi_l^i(t) \right\rangle = \sum \xi_l^p(t)\xi_l^i(t) = \delta(p-i) \quad (2.4)$$

Haar wavelet has been employed due to its simplicity. The description of Haar Wavelet in time domain is:

$$\emptyset(t) = \begin{cases} +1, & 0 \le t \le 1/2 \\ -1, & 1/2 \le t \le 1 \end{cases} \quad (2.5)$$

WPMCM transceivers are realized by an iterative method we can easily change the number of subcarriers and their bandwidth. By performing an additional iteration of 2-channel filter bank at all outputs the subcarriers number is doubled or more generally the number of subcarriers is given by

$$N=2^i \quad (2.6)$$

Where 'i' is number of iterations [4].

III. CHANNEL ESTIMATION

At the receiver, the transmitted signals are received from the multipath fading channel. In OFDM the ISI is removed by the guard interval whereas in WPMCM due to the carrier overlap in time domain, the overlap of symbols does not lead to ISI [5] [7].

So, the demodulated signal of the kth subcarrier can be represented as :

$$Y(k) = X(k)H(k) + V(k) \qquad 0 \le k \le N-1 \quad (3.1)$$

Where N is the number of sub-carriers, H(k) and V(k) represent the frequency transfer function of the channel and additive white Gaussian noise (AWGN) with zero mean and variance of σ_w^2.

In block-type pilot based channel estimation, channel estimation symbols are transmitted periodically, in which all sub-carriers are used as pilots [8]. If the channel is perfectly constant during the block, there will be no channel estimation error since the pilots are sent at all carriers. The estimation can then be performed by using either LSE or MMSE.

In this section we study the performance of the some channel estimation methods. We consider the popular least squares (LS) and minimum mean square error (MMSE) techniques which require less knowledge of the channel statistics [9].

A. LSE

The LS estimator for the channel impulse response H minimizes

$$\begin{aligned} J &= (Y\text{-}XH)^H (Y\text{-}XH) \\ &= (Y^H\text{-}H^H X^H)(Y\text{-}XH) \\ &= Y^H Y\text{-}Y^H XH\text{-}H^H X^H Y\text{-}H^H X^H XH \end{aligned} \quad (3.2)$$

For minimization of J we have to differentiate J with respect to H

$$\frac{\partial J}{\partial H} = 0$$

$$\hat{H} = X^{-1}Y \quad (3.3)$$

The time domain LS estimate of h is given by

$$h = F^H X^{-1} Y \quad (3.4)$$

B. MMSE

MSE (Mean Square Error) is expressed as

$$\begin{aligned} J(e) &= E[(H\text{-}\hat{H})^2] \\ &= E[(H\text{-}\hat{H})^H (H\text{-}\hat{H})] \end{aligned} \quad (3.5)$$

Where $\hat{H}$ is the channel estimate(with MMSE) and X^H denotes the Hermitian of the matrix X. Invoking the well-known orthogonality principle in order to minimize the mean square error vector e =H- $\hat{H}$ has to be set orthogonal by the MMSE equalizer to the estimators input vector Y.

$$\begin{aligned} E[((H\text{-}\hat{H})Y^H)] &= 0 \\ E[FhY^H] - ME[YY^H] &= 0 \end{aligned} \quad (3.6)$$

Considering the time domain channel vector h to be Gaussian and to be uncorrelated with the channel noise v we get,

$$\begin{aligned} R_{hY} &= E[hY^H] \\ &= E[h(XFh+v)^H] \\ &= R_{hh} F^H X^H \qquad (\text{as } E[hv^H]=0) \end{aligned} \quad (3.7)$$

Now,

$$\begin{aligned} F(R_{hY}) &= R_{hh} X^H \qquad (\text{as } FF^H = I) \\ R_{YY} &= E[YY^H] \\ &= E[(XFh+v)(XFh+v)^H] \\ &= XFR_{hh}F^H X^H + \sigma^2 I_V \end{aligned} \quad (3.8)$$

Therefore,

$$F(R_{hY}) = M(R_{YY}) \text{ where } M = F R_{hY} R_{YY}^{-1} \text{ and } \hat{H} = F R_{hY} R_{YY}^{-1} Y$$

The time domain MMSE estimate of h is given by

$$\hat{h} = R_{hY} R_{YY}^{-1} Y \quad (3.9)$$

IV. SIMULATION RESULTS

In this section simulation results are presented which show the performance comparison of WPMCM and OFDM in terms of BER in various wireless channels. The both OFDM and WPMCM systems are developed, analyzed, and simulated in Matlab. The performance results of the system are done in AWGN channel. Simulation parameters are shown in Table 1. The results of LS and MMSE estimation techniques are shown below:

Fig 4 shows the Mean square error Vs SNR for the LS and MMSE techniques in OFDM. Fig 5 shows the Mean square error Vs SNR for the LS and MMSE techniques in WPMCM. In both cases results shows that MMSE is clearly better option when compared to LS.

Table 1

Simulation Parameters

Parameters	OFDM	WPMCM
Type of modulation	QAM and BPSK	QAM and BPSK
No of sub carriers	16	16
bits per symbol	4	4
Channel	AWGN	AWGN
No of FFT points	64	-
Wavelet used	-	Haar

Fig 6 shows the performance comparison of OFDM and WPMCM based on BER Vs SNR plot. The modulation technique used here is 4-QAM.

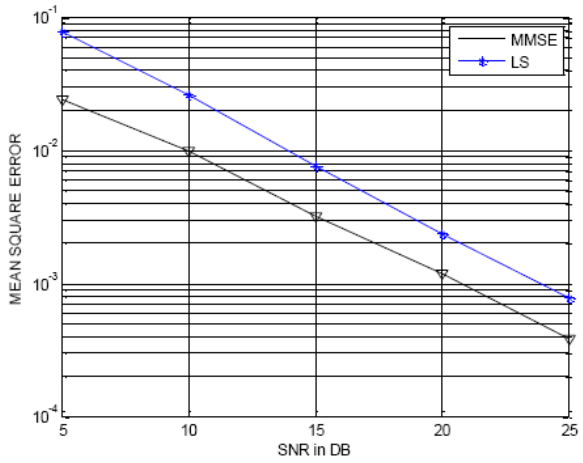

Fig. 4 : MSE Vs SNR for an OFDM system with LS & MMSE estimators

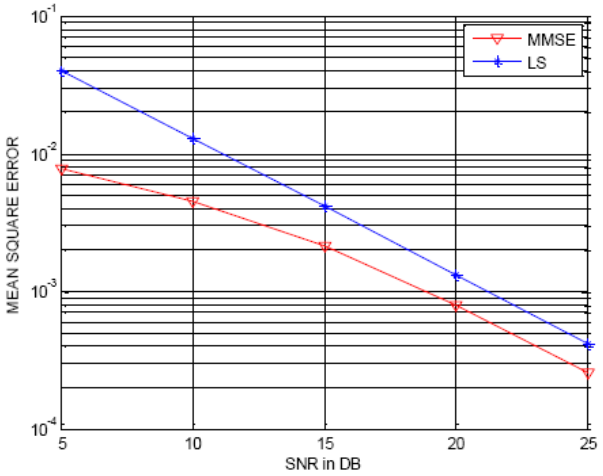

Fig. 5 : MSE Vs SNR for a WPMCM system with LS & MMSE estimators

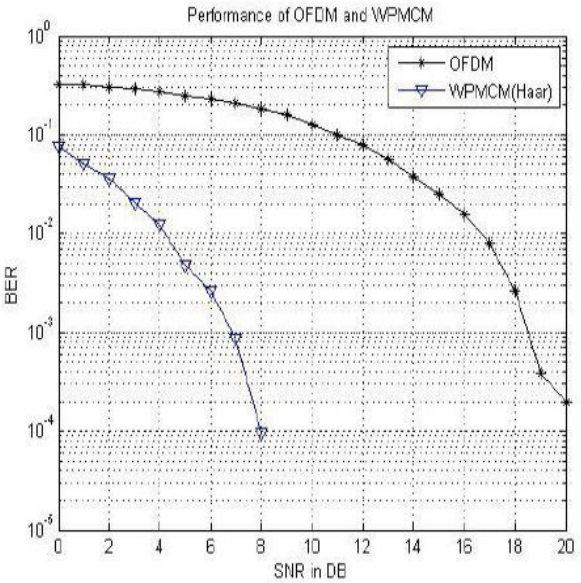

Fig. 6: BER performance of 16 sub-carrier OFDM and WPMCM

V. CONCLUSION

In this paper we present the performance analysis of WPMCM as an alternative for OFDM. The results in terms of BER show that WPMCM system is superior to OFDM system. There is almost 18 dB gain at a BER of 10^{-2} in OFDM systems when using HAAR wavelet based WPMCM system instead of OFDM system. Simulation results of LS and MMSE for both OFDM and WPMCM show that MMSE is better than LS.

WPMCM system and OFDM system have nearly the same complexity according to the number of carriers. However, wavelets allow more flexibility in the

system design. The performance results indicate that WPMCM is a viable alternative to OFDM but at the cost of higher complexity of equalization. Although, OFDM offers a low complexity structure than WPMCM, however, the use of CP reduces its spectral efficiency and wastes transmit power.

The research can be extended to MIMO case and performance can be analyzed under different fading environments.

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Industrial Power Automation Using Power Line Carrier Communication

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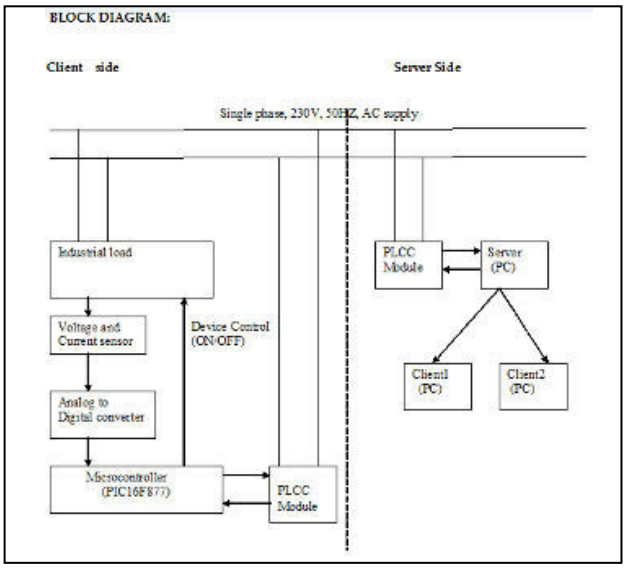
Abstract - This system describes the design and implementation of power line carrier communication to control the switching on and off of the loads in an industry automatically without manual monitoring of the load. The loads can be switched off using a lab view visualized program setting a threshold value of power. Once the set threshold value is reached control to switch off the load that consumes more power is switched off by passing bits for that at the zero crossings of the 230V AC supply. This system design uses a PIC microcontroller, power line carrier communication modem, voltage and current sensors and relay switches. Meanwhile, through the application of power line carrier communication anddetermining parameters to find power i.e. voltage and current values are determined through respective sensors and industrial power automation using power line communication system is developed. Live monitoring of voltage and current parameters is possible and controls the power consumption of load that consumes more power reducing the current bills. This technology is useful in communicating through the power lines and no special wires are required for controlling loads in an industry.

Keywords - *PLCCModule,PIC,Threshold,Labview.*

I. INTRODUCTION

For responding to the recent rapidly increasing trend of petroleum price, expecting the reduction of power generation cost, and achieving the goal of energy conservation and carbon reduction, many governments in the world are trying all the efforts by applying information and communication technology (ICT) into the development of green energy to promote energy utilization efficiency. Industrial power consumption tends to grow in proportion to the increase in the number of large-sized electric home appliances. By using power line carrier communication (PLCC) technology, electric industrial appliances can be controlled and monitored through domestic power lines. The PLCC module and a microcontroller into a power outlet to switch the power of the socket on/off and to measure the power consumption of plugged-in electric industrial appliances. We have also designed an lab view visualizes program user interface, thus allowing the user to easily control and , monitor the electric appliances by means of the PC. PLC is like any other communication technology whereby a sender modulates the data to be sent, injects it onto medium, and the receiver de-modulates the data to read it. the major difference is that PLC does not need extra cabling, it reuses existing wiring. Considering the pervasiveness of power lines, this means with PLC, virtually all line-powered devices can be controlled or monitored. The main advantage with power-line communication is the use of an existing infrastructure.

The new ATL90 series Embedded PLC modem series is based on the Direct Sequence Spread Spectrum Technology. The new technology in Power Line Carrier (PLC) communication is well known for its high immunity to electrical noise persistent in the power line. With the new solution, the form factor of the PLC modem is further reduced and its cost lowered. The Embedded PLC Modem is in the form of a ready-to-go circuit module, which is capable of transferring data over the power cable at the low voltage end of the power transformer of a 3-phase/ 4-wire distribution network Applications of the Power Line Modem include status monitoring, control and data communication of devices connected on the power line, such Home Automation, Lighting Control, HVAC control, Low Speed Data Networks, Automatic Meter Reading, Signs and Information Display, Fire and Security Alarm, ……., and so on



II. HARDWARE DESCRIPTION:

The Hardware section comprises of two section namely the client and server side. The client side includes voltage and current sensors, microcontroller (PIC 16F877a), analog to digital convertors and relay switches connected to industrial loads.Theplcc modem is used for communicating the determined parameters(voltage & current) from the client side to the server side. The server side includes plcc modem connected to a pc where live monitoring of the power is possible.

Now let us see about the client side briefly

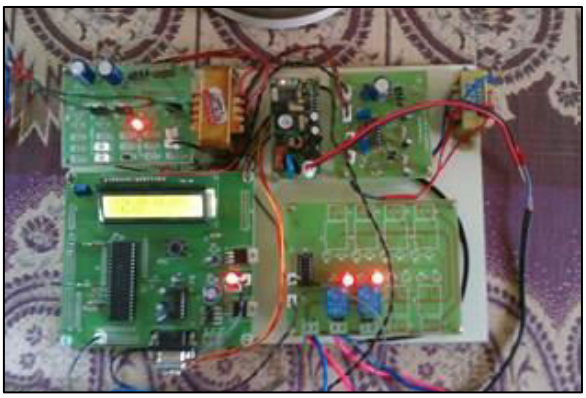
Microcontroller : The PIC16F877a CMOS FLASH-based 8-bit microcontroller featuring 200ns instruction execution, 256 bytes of EEPROM data memory, self programming, a LCD, 2 COMPARATORS, 8 CHANNELS OF 10-BIT ANALOG –to – DIGITAL(A/D) convertor, 2 capture/compare/PWM functions, a synchronous serial port that can be configured as either 3- wire SPI or 2-wire I2C bus, a USART, and a Parallel Slave Port. All of these features make it ideal A/D application in automotive, industrial, application, and consumer application.

Current transformer : A current transform is a devices for measuring a current flowing through a power system and inputting the measured current to a protective relay system. Electric power distribution system may require the use of a system malfunctions. Current transform and current sensor are well known in the field off electronic circuit breakers, providing the general function of powering the circuit.

Voltage transformer : The standards define a voltage transformer as one in which “the secondary voltage is substantially proportional to the primary voltage and differs in phase from it by an angle which is approximately zero for an appropriate direction of the connection.”This, in essence, means that the voltage transformer has to be as close possible to the “ideal” transformer. In an “ideal” transformer, the secondary voltage vector is exactly opposite and equal to the primary voltage vector, when multiplied by the turns ratio.

Relays **:** A relay is an electrically operated switch. Current flowing through the coil of the relay creates a magnetic field which attracts a lever and changes the switch contacts. The coil current can be on or off so relays have two switch positions and most have double throw (changeover) switch contacts as shown in the diagram. Relays allow one circuit to switch a second circuit which can be completely separate from the first.

PLCC module : A pair of Embedded PLC Modems connected on the power line can provide low speed bi-directional data communication at a baud rate of 300/600 bps. It is built in a small form factor that can be easily integrated into and become part of the user's power line data communication system. The modules provide bi-directional half-duplex data communication over the mains of any voltage up to 250v a. c., and for frequency of 50 or 60 Hz. Data communication of the modules is transparent to user's data terminals and protocol independent; as a result, multiple units can be connected to the mains without affecting the operation of the others. The use of DSSS modulation technique ensures high noise immunity and reliable data communication. There is no hassle of building interface circuits. Interface to user's data devices is a simple data-in and data-out serial link. It has a built-in on board AC coupling circuit, which allows direct and simple connection to the mains



The ATL90115 series Embedded PLC Modem is a ready-to-go circuit module, which is capable of transferring data over the power cable at the low voltage end. A pair of Embedded PLC Modems connected on the power line can provide low speed bi-directional data

communication at a baud rate of 300 bps. It is built in a small form factor that can be easily integrated into and become part of the user's power line data communication system. The PLC modem is based on the Direct Sequence Spread Spectrum Technology, which ensures high noise immunity and reliable data communication. The modules provide bi-directional half-duplex data communication over the mains of any voltage up to 250v a. c., and for frequency of 50 or 60 Hz. Data flow through PLC modem as if it is a channel and therefore it is transparent to the Data Devices. As a result, with user's proper addressing and communication protocol, multiple units can be connected to the mains without affecting the operation of one another. There is no hassle of building interface circuits. It has a built -in on board AC coupling circuit, which allows direct and simple connection to the mains. Interface to user's data devices is a simple data -in and data-out serial link. Power to the PLC Modem circuit module is a single +12v DC supply.

Server Side : In the server side, the transmitted bits from the client side is received anddemodulated by the plcc module in the server side. A visualized labview front panel done in the pc is used to input threshold limits for the votage and current parameters. Live monitoring of the power consumed by the loads in the industry can be viewed in this pc. Once the threshold limits are crossed, the control signal to switch off the load is automatically sent from pc to client side loads through the power line carrier communication. Loads are switched off automatically by this way.

III. CONCLUSION :

PLC solutions may be seen as complementary or alternative solutions to traditional fixed line networks, wireless networks and VDSL networks. PLC bandwidths are set to increase, the Homplug AV standard is being considered for broadcasting digital television.

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Phase Unwrapping of Images

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Abstract - In this paper, we present the effect of discontinuities of phase in the process of unlocking the locked signal which is unfortunately obtained from a particular application. The locked or the wrapped image is never desired. The unlocking or the unwrapping of the wrapped image is required so that information regarding deformation of a geographical location or a structure can be used for the benefit of mankind.

Keywords - *Wrapped phase, InSAR images, phase discontinuities, phase jumps.*

I. INTRODUCTION

Phase unwrapping is a basic problem in signal processing. Phase unwrapping is the process of recovering the original signal from the wrapped image different methods to achieve unlocked outputs from locked inputs have been discussed in [3] and [4]. They can be subdivided into several different categories, depending on, e.g., if they work locally or globally. Network flow, branch-cut, minimum norm methods are explained in [5]-[7].. Medical, military and industrial applications require the extraction of the unwrapped phase signal from the wrapped signal. The phase which is obtained has 2π phase jumps, which results in the formation of the wrapped image. [1][2] This wrapped phase is unusable until the phase discontinuities are removed . An interferometer is an instrument used to interfere waves . Interferometry refers to a family of techniques in which electromagnetic waves are superimposed in order to extract information about the waves. Interferometry is an important investigative technique in the fields of astronomy, fiber optics, engineering metrology, optical metrology, oceanography, seismology, quantum mechanics, nuclear and particle physics, plasma physics, remote sensing and biomolecular interactions Interferometry makes use of the principle of superposition to combine or separate waves in a way that will cause the result of their combination to have some meaningful property that is diagnostic of the original state of the waves. This works because when two waves with the same frequency combine, the resulting pattern is determined by the phase difference between the two waves—waves that are in phase will undergo constructive interference while waves that are out of phase will undergo destructive interference. Most interferometers use light or some other form of electromagnetic wave. This paper explains a simple algorithm for wrapping and unwrapping of one-dimensional images. This paper is organized as follows, Section 2 explains two dimensional explains two dimensional phase unwrapping. Section 3 discusses the effects of phase discontinuities and concludes the paper.

II. TWO-DIMENSIONAL PHASE UNWRAPPING [8][9]

A wrapped phase image obtained from a simulated InSar is shown in Fig.1. Images like in Fig.1 do not display much information when seen directly by human eyes. But, such images of geographical locations or physical structures convey a lot of information when processed.

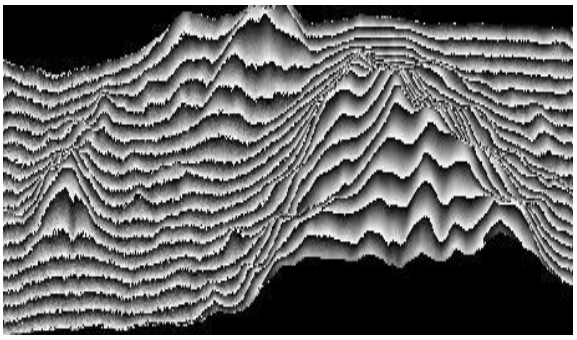

Fig.1: Wrapped phase image obtained from a simulated InSAR [8]

In this paper, a simulated image is considered as shown in Fig.2. This same image is then plotted as a surface in Fig.3.

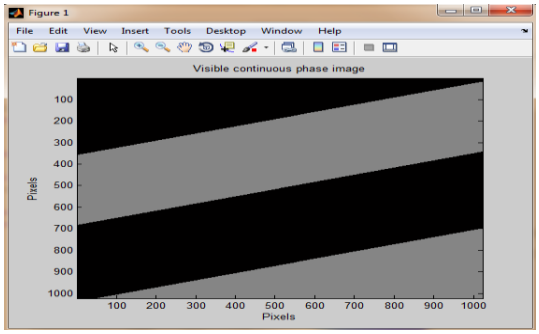

Fig. 2 : Continuous phase image

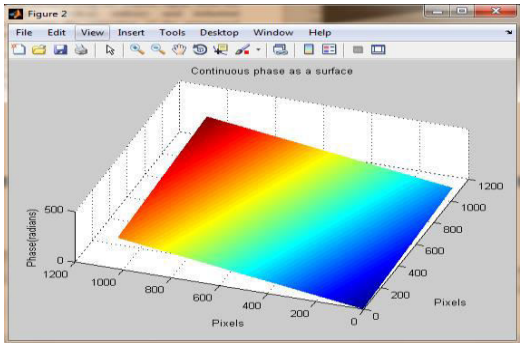

Fig. 3 : Image in Fig.2 plotted as a surface.

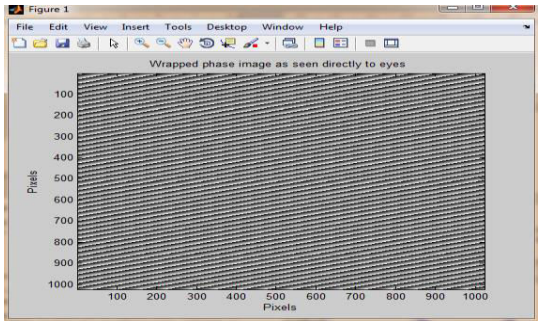

Fig. 4: The original image as in Fig. 2 is locked.

2.1 The unwrapping process[1][2]

The image which is locked must be unlocked to make it usable for applications.

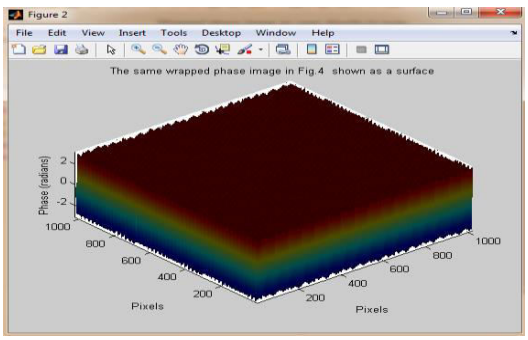

Fig. 5: Image in Fig.4 plotted as a surface

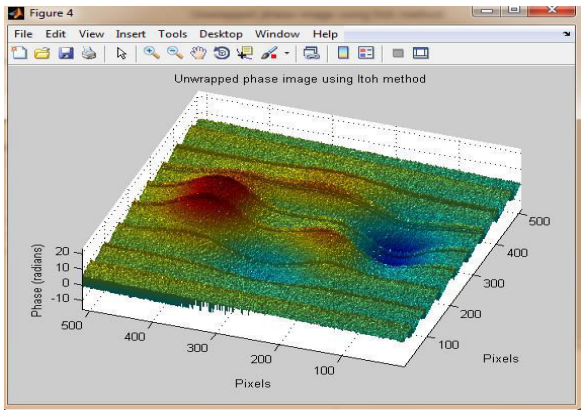

Fig. 6 : Image is unwrapped

III. EFFECTS OF PHASE DISCONTINUITIES

There can be several problems affecting the unwrapping of image like those faced with the unwrapping of signals. One of it is the phase being not continuous. Let us consider a computer generated image shown in Fig. 7 below.Fig. 7 is an image shown as a visual array.

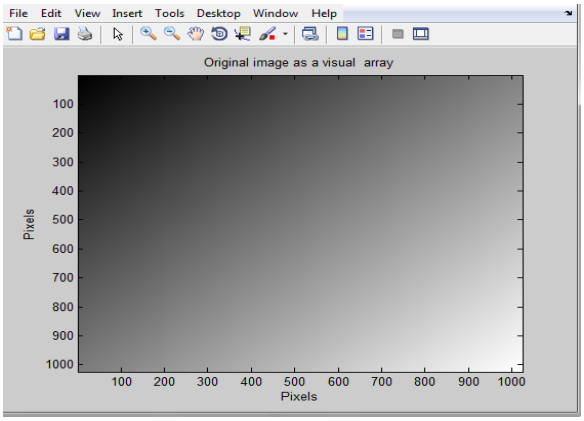

Fig.7: A computer generated image with phase change =12

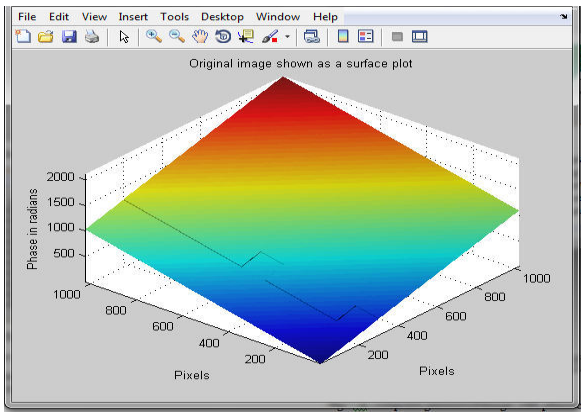

Fig. 8: The Fig.7 is displayed as a surface plot.

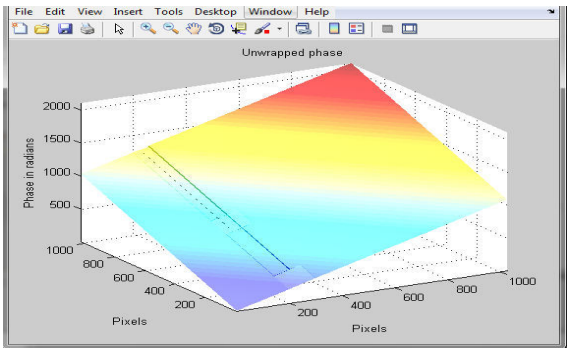

Fig. 9 : The unwrapped phase image by overcoming the phase discontinuities.

IV. CONCLUSION:

Phase unwrapping involves a number of steps, some of which may lead to undesired results due to phase discontinuties. Thus, it is seen that these factors should be in exact proportion in order to have the exact unlocking of the signal.

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Reduction of Coupling between Microstrip Array Antennas using Electromagnetic Band Gap structure

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Abstract - Electromagnetic Band-gap (EBG) or High Impedance Surface (HIS) structures are becoming more and more utilized in the microstrip antennas and particularly to reduce the mutual coupling between the radiate elements or arrays antennas. In this paper, the band-gap feature of High Impedance Surface Mushroom-like Structure is introduced into a ground plane of the antenna arrays system to reduce the mutual coupling for 10GHz frequency application. A drastically mutual coupling reduction is reached -45 dB at 10GHz.

Keywords - *Electromagnetic band-gap (EBG), High Impedance Surface, HIS, microstrip array antennas, mutual coupling, surface wave.*

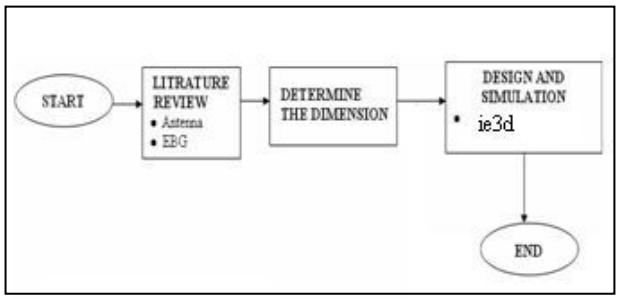
I. INTRODUCTION

The research in the field of electromagnetic band gap or well known as EBG structure has becoming attractive in antenna community. This structure has a unique property such as the ability to suppress the propagation of surface wave in specific operating frequency defined by the EBG structure itself. The electromagnetic band gap (EBG) structures are periodical metallic particles inserted in a dielectric host medium [1-4] and backed by a metallic ground plane. The mushroom-like HIS, shown in Fig. 1(a) was developed by Sivenpiper firstly for the microwave frequency.

The major characteristic of EBG structures is to exhibit band gap feature in the suppression of surface-wave propagation [1]. Since the mutual coupling between the antenna elements and arrays is principally carried by the wave surface, the use of HIS can help to attenuate their level if the topology and implementation are carefully designed.

The electromagnetic band gap structure always used as a part of antenna structure in order to improve the performance of the antenna especially for improves the gain and radiation pattern. In this paper, microstrip antenna is used due to the advantages such as easy and cheap fabrication, light weight, low profile and can easily integrated with microwave circuit. This paper involves the investigation of mushroom like EBG structure and the integration of the EBG structure with antenna design through the simulation. The simulation is done by using ie3d. In order to validate our study a Four-Element array antenna structure is chosen as a unit element. The distance between two neighbor arrays is $2\lambda 10GHz$, where λ10GHz is the free space wave length.

From the simulation done, most of the antenna which has been incorporated with EBG structure show the enhancement of the performance in term of radiation pattern, gain and return loss, S11. The 1 dB gain increment is noticed for microstrip array antenna with incorporated with EBG structure. The radiation pattern also improves where the side and back lobes are decreasing by using EBG structure in the ground plane of the antenna. The steps involved in this paper is given in the form of flow chart.



Flow chart

II. MICROSTRIP ANTENNA

A microstrip patch antenna is a narrowband, wide-beam antenna fabricated by etching the antenna element

pattern in metal trace bonded to an insulating substrate. Because such antennas have a very low profile, are mechanically rugged and can be conformable, they are often mounted on the exterior of aircrafts and spacecrafts, or are incorporated into mobile radio communications devices. Microstrip antennas have several advantages compared to conventional microwave antennas therefore many applications cover the broad frequency range from 100 MHz to 10 GHz. Some of the principal advantages compared to conventional micrwave antennas are:

- Light weight, low volume, end thin profile configurations which can be made conformal
- Low fabrication cost.
- Linear, circular and dual polarization antenna can be made easily
- Feed lines and matching networks can be fabricated simultaneously with the antenna. However microstrip antennas also have limitations compared to conventional microwave antennas.
- Narrow bandwidth and lower gain
- Most microstrip antennas radiate into half space
- Polarization purity is difficult to achieve
- Lower power handling capability.

III. SOFTWARE SELECTION FOR SIMULATION

The software used to model and simulates the Microstrip antenna was Zeland Inc's IE3D. IE3D is an integrated full-wave electromagnetic and simulation package based on the method of moments for the analysis and design of 3D (threedimensional) microstrip antenna, high frequency printed circuits and digital circuits such as MMICs and high speed printed circuit boards (PCBs). It can be used to calculate and plot RL (Return Loss), VSWR (Voltage Standing Wave Ratio), Radiation pattern (Azimuth and Elevation), Smith chart and various other parameters.

IV. DESIGN PROCESS OF ANTENNA

Through all the design process, air gap has been used to build the antenna structures. The reason for choosing this is because by using certain dielectric substrates the efficiency of the antenna will be reduced. secondly it is very easy to construct the antenna. Based on the antenna knowledge concentration has been put on the linearly polarized transmitted signal, because the bandwidth of the linearly polarized antenna is greater than the circularly polarized antenna. Linear polarization is preferred as compared to circular polarization because of the convenience of a single feed than a double feed. Moreover the construction of linearly polarized rectangular patch antenna or Square patch antenna is simpler than the other polarization configurations. In the present work, The Transmission line model has been used to design a rectangular or square patch antenna.

Design Calculation Formulae

The operating frequency fr

Thickness of the dielectric medium,

$$h \le 0.3 \times \frac{c}{2 \times \prod \times f_r \times \sqrt{\varepsilon_r}}$$

Thickness of the grounded material alumina,

$$h \le 0.3 \times \frac{c}{2 \times \prod \times f_r \times \sqrt{\varepsilon_r}}$$

Width of metallic patch,

$$W = \left(\frac{c}{2 \times f_r}\right) \times \left(\frac{\varepsilon_r + 1}{2}\right)^{\frac{-1}{2}}$$

Length of metallic patch, L

$$L = \frac{c}{2 \times f_r \times \sqrt{\varepsilon_{reff}}} - 2\Delta l$$

Where,

$$\Delta l = 0.412 \times h \times \left[\frac{\left(\varepsilon_{reff} + 0.03\right) \times \left(W + 0.264h\right)}{\left(\varepsilon_{reff} - 0.258\right) \times \left(W + 0.8h\right)}\right]$$

$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \times \left(1 + \left(\frac{12 \times h}{W}\right)\right)^{\frac{-1}{2}}$$

Now the designed values are substituted in the IE3D software. Then the schematic is drawn using MGRID in that software and the results areobtained using Modua curve.

V. HIS STRUCTURE

Electromagnetic Band Gap (EBG) always referred as photonic band gap (PBG) surface or high impedance surface. This structure is compact which has good potential to build low profile and high efficiency antenna surface. The main advantage of EBG structure is their ability to suppress the surface wave current. The

generation of surface waves decreases the antenna efficiency and degrades the antenna pattern. Furthermore, it increases the mutual coupling of the antenna array which causes the blind angle of a scanning array. The feature of surface-wave suppression helps to improve antenna's performance such as increasing the antenna gain and less power wasted when reducing backward direction.

High Impedance Surface has a zero degres phase reflection coefficient within the band-gap and presents a very high effective impedance surface which is opposed to the case of a perfect conducting surface. Fig. 1 presented the HIS structures called "Mushroom-like" and "Fork-like patches" and the unit cells dimensions. The operation mechanism of the EBG structure can be explained by an LC filter array: the inductor L results from the current flowing through the vias and the capacitor C due to the gap effect between the adjacent patches. These values as well as the frequency band gap could be calculated using the following references [4-5].

$$BW = \frac{\Delta\omega}{\omega} = \frac{1}{\eta}\sqrt{\frac{L}{C}}$$

Where

$$\omega = \frac{1}{\sqrt{LC}}$$

And η=120π is the free space impedance.

The mushroom like EBG structure looks like a rectangular structure placed at regular intervals in the ground plane of the array antenna structure.

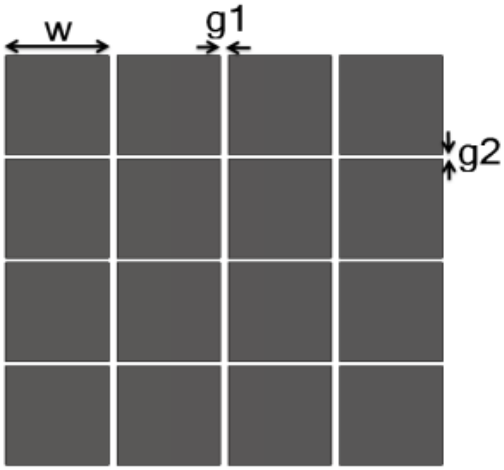


Fig. 1 : *Mushroom cells.The dimensions are W=0.1* λ10GHz and g1=g2=0.02 λ10GHz.

VI. FOUR ELEMENTS ARRAY

Fig. 2 shows the designed array antenna. It includes four patches with distances D in both directions [7]. The length and width of the single element are determined using the formulas. The network includes a center line of 100 Ω fed at its center by an ideal 50Ω source. In each one of the splitting points there are two 100Ω lines going to the patches. Fig. 3 shows ie3d simulated results of the array antennas. The array antenna has a resonant frequency of 10 GHz and sems to be well matched as shown by the return loss of the array antennas Fig. 3(a). Fig. 3(b) shows that the radiation pattern and the structures have a 6% bandwidth.

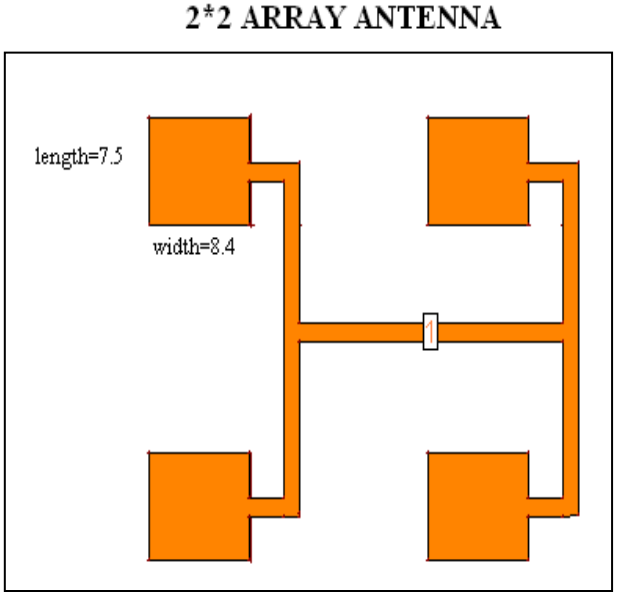
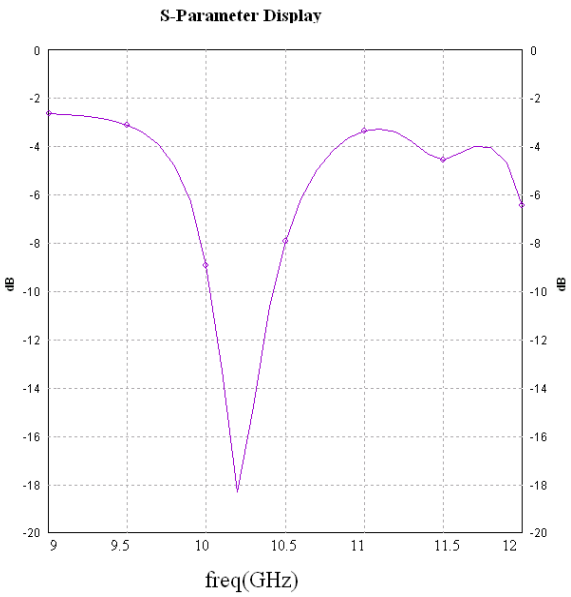


Fig. 2 : The designed array antenna with four elements

S-Parameter Magnitude in dB



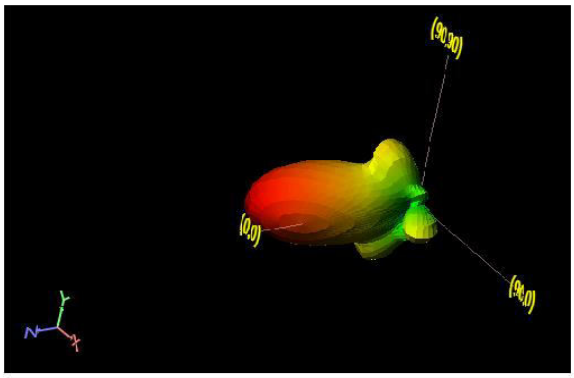


Fig. 3: The simulated characteristics of array antenna a) return loss and b) radiation pattern

VII. REDUCTION OF MUTUAL COUPLNG BY USING EBG

The simulated results of four element array antenna shows the result of about -18 dB at 10 GHz which show strong mutual coupling due to the pronounced surface waves. The mushroom like EBG patches are introduced in the ground plane of the array antennas to reduce the mutual coupling, as shown in Fig. 4.

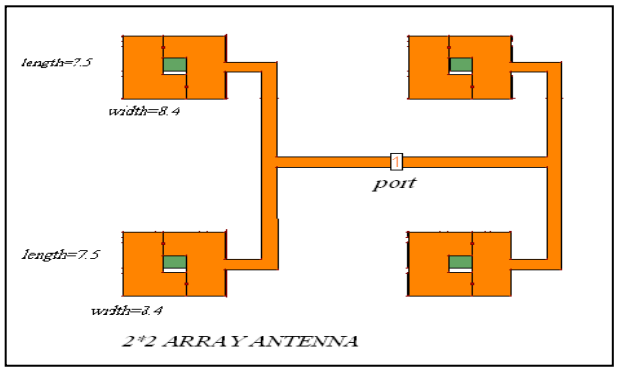


Fig. 4: Array antennas with EBG in the ground plane

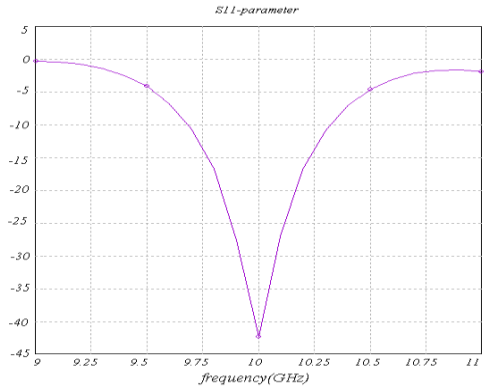


Fig. 5: S- Parameter display of Array antennas with EBG strucuture

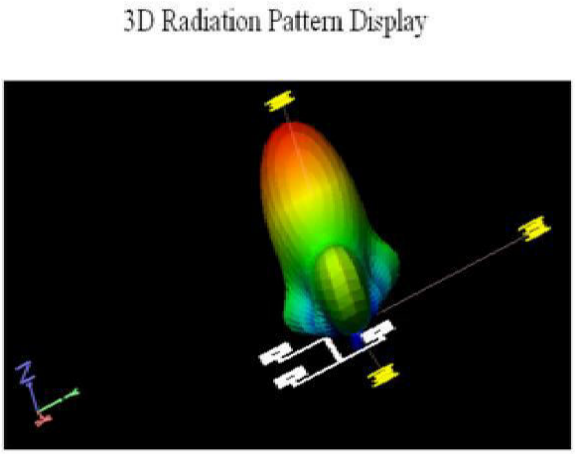


Fig. 6: Radiation pattern of Array antennas with EBG in the ground plane

Fig. 5 shows ie3d simulated results of the microstrip arrays antennas on a dielectric substrate with h=1.6 mm, and εr =2.5, the arrays' size are given in Fig.4. The Mushroom-like are introduced in the ground plane of the arrays antennas to reduce the mutual coupling. We observed that without EBG structure, there is a mutual coupling of -18 dB. If the EBG structures are employed, the mutual coupling level changes. When the Mushroom-like EBG is used, the mutual coupling is reduced and a coupling of -45 dB is noticed at 10 GHz. Fig. 6 shows the radiation pattern of the 2x2 array antenna.

VIII. CONCLUSION

In this paper, we studied high impedance surface namely mushroom like EBG structure and applied them to reduce the mutual coupling effect in the ground plane of the arrays antennas. All the simulations are analyzed by ie3d simulation software. The effects such as the finite size ground plane which diffract the surface waves, the lateral coupling waves at short distances and the measurement conditions must be taken in to account in order to validate our simulations. Presently, a set of configuration circuits are realized and will be characterized. By the simulation, a mutual coupling reduced of about -10 dB is obtained by using HIS barrier technique.

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A Fully Integrated Neural Signal Acquisition Amplifier for Epileptic Seizure Prediction

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Abstract - This paper deals with the design of low power low noise neural signal amplifier for Epileptic Seizure Prediction. The advent of Micro-electro Arrays has driven the need for implantable electronic circuitry to detect those Extracellular neural signals (ENG). We proposed a preamplifier of fully differential Low Noise Amplifier (LNA) with g_m boosting in order to enhance the gain as well as reduce the power consumption. Low frequency high pass function has been realized with anti-parallel Diode connected PMOS. Simulation results shows that the input referred noise is 1.24µVrms from 100Hz to 5 KHz, mid-band voltage gain of 44.6dB, and the power consumption is 18.74µw. A new signal processing circuit has been designed extract the seizure onset. The results are validated using Cadence spectre simulator with 180nm technology. Simulation results show that this implantable amplifier is suitable for Epileptic seizure prediction.

Keywords: *Epileptic Seizure, NSA, pseudo resistor, Low frequency High Pass Function (LFHPF)*

I. INTRODUCTION

Early prediction of severe epilepsy may helpful for the patients to escape from fatal accidents. Much research is being done on Epileptic seizure prediction using EEG Signals. While using EEG signals many false positives are reported. So, the better alternate for this system is to use implantable devices recording ENG signals. ENG signals are small in amplitude from 5µV to 500µV and have a low frequency spectrum of 100Hz to 5 KHz[1]. However in practice, the distance of Micro-electrode arrays (MEA) are difficult to control and the resulting ENG is very small requiring a LNA for signal amplification cum detection.

The overall block diagram for Epileptic Seizure detection is shown in figure1. Output from the ENG signal acquisition amplifier (NSA) is directly taken as clinical data, further the signal is sent through a proposed simple signal processor to extract the seizure onset. Later the extracted feature will be compared with the reference neural signal Potential (Vsyn) using high speed latch comparator.[2]. The composite Neural signal consists of large DC offset due to the body fluid where the MEA resides and Electromyography (EMG) noise, Power Line frequency interference. The DC offset and EMG noise can be removed by Low frequency High Pass Function [3].

MOSFET based design for low frequency bio-medical application has inherent flicker noise, it cause poor SNR. Some of the solutions to reduce the flicker noise are chopper stabilization and Auto-zeroing, both cases consumes more power, it is not advisable for implantable applications [4,5]. The flicker noise is dominating in the PMOS. The flicker noise and the valid signals are having the same 150Hz spectrum, so the transistors made large to increase its transconductance (g_m) [6], thereby the noise is eliminated. The proposed LNA with sub-threshold PMOS input pair with gm-boosting shows valid results

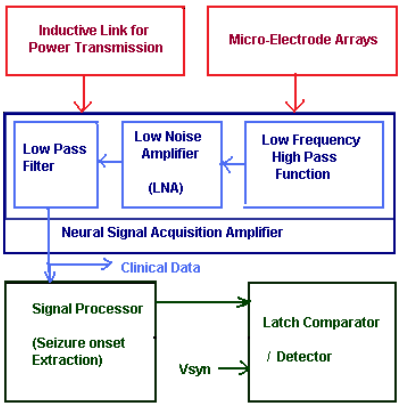

Figure1. Overall Block Diagram of Epileptic Seizure Detection

This LNA has fully differential topology in order to eliminate the coherent noise. The design of low frequency High pass function is challenging one. In our proposed Circuit Anti-parallel Diode connected PMOS is used as Pseudo resistor. It consumes less power and exhibits bilinear characteristics. The differential output is converted into single ended by the high linear OTA-C filter, which is nothing but a Low pass Filter in this design[6].

The section1 gives brief Introduction of this Work, section II explain the inductively coupled power supply for implantable circuits, section III explains the realization of Pseudo-resistors, section IV describes the functionality of low frequency high pass function, section V explains the functional details of LNA, Section VI reveals the LNA Noise Analysis, Section VII explains about the High Linear Low Pass filter, section VIII explains a new signal processing circuit and Section IX Concludes the work with the obtained parameters.

II INDUCTIVE COUPLED RAIL-TO-RAIL SUPPLY

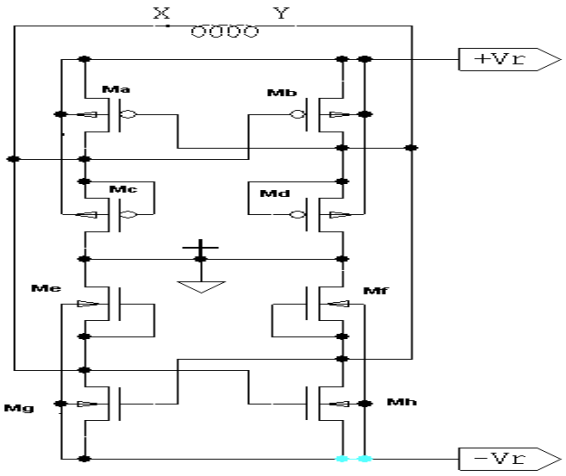

Figure 2(a) Rail-to-Rail Rectifier Circuit

For the past few years, high-performance implantable bio-medical ICs plays a major role in modern medicine. With the advent of nanotechnology, Battery based circuits are not entertained for implantable applications. Nowadays, inductively coupled link is more desirable method for patient, because of its high power transfer efficiency and safety. Bio-medical amplifiers shows good result, when using rail-to-rail power supply. In the proposed method, the sinusoidal output from the secondary coil is applied between the terminals X and Y. When potential on side X is more than that of Y, the transistors Mb,Mc,Mf and Mg are forces to shut-off while Ma,Md,Me and Mh are turned on. Therefore, we can get positively and negatively unidirected supply from terminals +Vr and –Vr respectively for both positive and negative half cycles. The unidirected supply is passed through a capacitor filter to remove its ac contents (ripples). By using a suitable regulator we can a dc for the circuit. For the regulation, zener diode is not preferred because of its parasitic capacitance. Some CMOS circuits based on voltage reference may be used

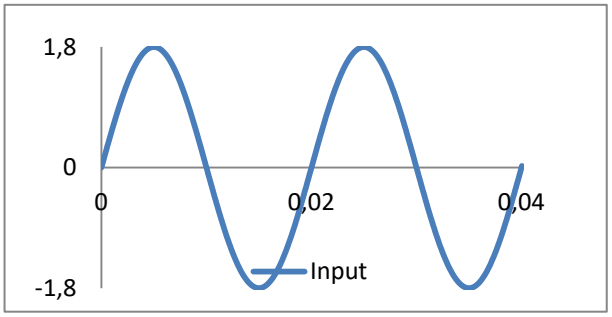

Figure 2(b) Input waveform

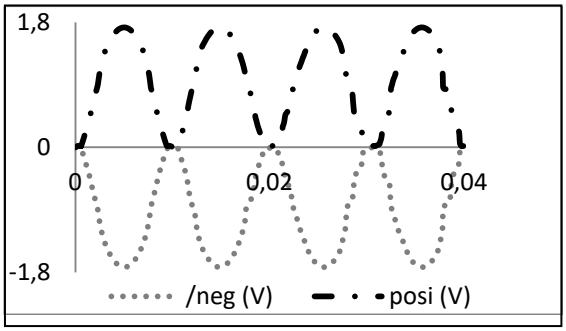

Figure 2 (c) Output waveform

III. PSEUDO-RESISTORS

The Pseudo-resistors plays a vital role in the realization of low frequency high pass function, in order to avoid large on-chip capacitor resulting high power consumption and poor SNR, The resistors of the order of several Giga- ohms are needed for this circuit[7]. There are six different structures as shown in the figure3.The linear variation of current for each structure is plotted for comparison. The fig 3. (a,b) shows the uni-linear, resulting noise disturbance is more.

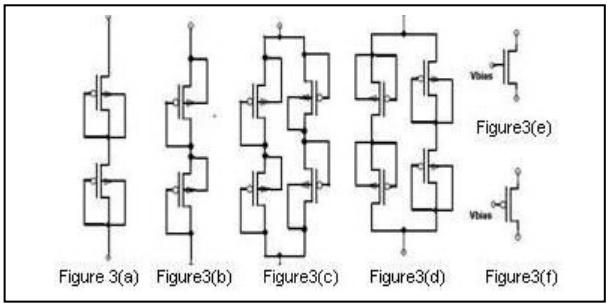

Figure3. Different Structures of Pseudo-Resistor

The transfer characteristics for single and anti-parallel connected is shown in the figure4. From this I-V curve we can understand the anti-parallel connected (DoubDio & DoubSG) pseudo resistor exhibits bilinear characteristics. The figure3.(e,f) uses sub-threshold PMOS and deep-depletion NMOS respectively. In both cases, it needs additional biasing for tuning purpose. For implantable applications, the supply is applied externally through inductive coupling. Therefore the design with large number of biasing is not preferred. Figure3. (c,d) shows bilinear characteristics and doesn't require additional biasing for tuning purpose. Out of these two, Figure3.c is better suited for this application due to high linearity. The linear resistance curve is shown in figure5.

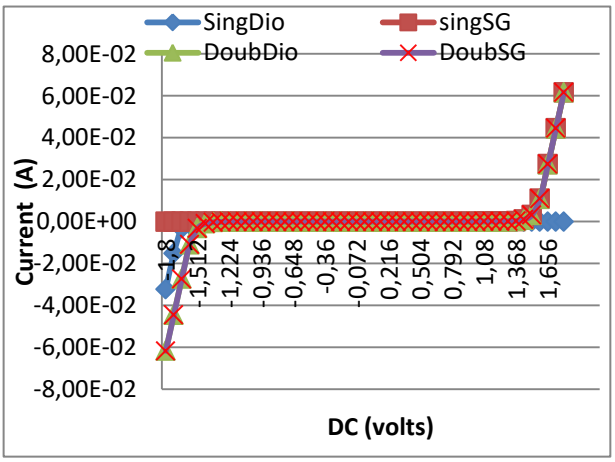

Figure3.Transfer characteristics of pseudo-resistors

The drain current of PMOS transistor operating in sub-threshold region is

$$I_d = I_o\left[1 - exp\left(\frac{V_d}{V_t}\right)\right]\exp\left[\frac{V_g - V_{th} - V_{eff}}{nV_t}\right] \quad (1)$$

Where, I_d = drain Current; V_d = source- drain voltage; V_t = thermal voltage; V_{th} = threshold voltage; n = sub-threshold swing parameter; V_g = gate-source voltage.

The differential resistance ∂R can be obtained by differentiating I_d with respect to V_d.

$$\frac{\partial I_d}{\partial V_d} = \frac{1}{R_{out}} = \frac{I_o}{V_t}.\exp\left[\frac{V_g - V_{th} - V_{eff}}{nV_t}\right].exp\left(\frac{V_d}{V_t}\right) \quad (2)$$

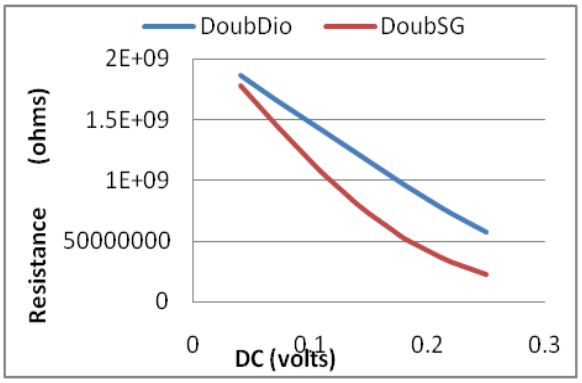

Figure5. Linearity Comparison of Anti-parallel Diode connected and Source-Gate connected

IV. LOW FREQUENCY HIGH PASS FUNCTION

This circuit serves two purposes. First, it avoids the DC voltage value of the body fluid where the MEAs are placed, because Dc voltage may saturate the output of LNA. Second, it removes the EMG noise spectrum which resides within 100Hz. This circuit is built by the pseudo-resistors, in order to avoid the high power consumption. The mid-band gain value is set by the capacitors C1 and C2[8]. For bio-medical implantable applications, mid band- gain normally chosen by the ratio of c1 and c2 as 50. We can use either open loop or closed loop configuration as shown in figure.6.

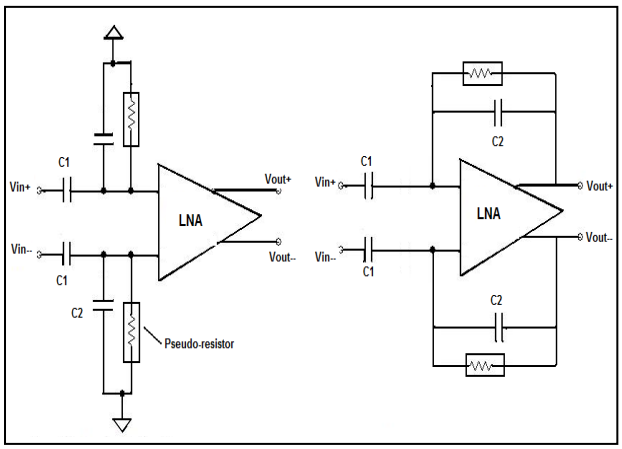

Figure6. Open Loop and Closed Loop Configuration

Simulation results show that the open loop configuration is better due to the high gain and Low Power consumption. No stability problem arises around the region of interest.

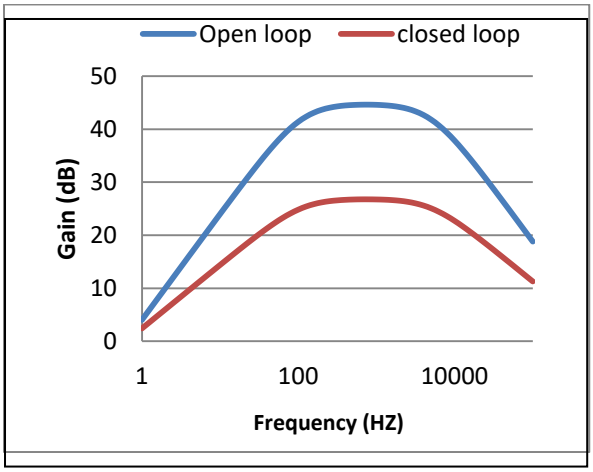

Figure 6(a). Gain Comparison between open loop and closed loop configuration

V. LOW NOISE AMPLIFIER (LNA)

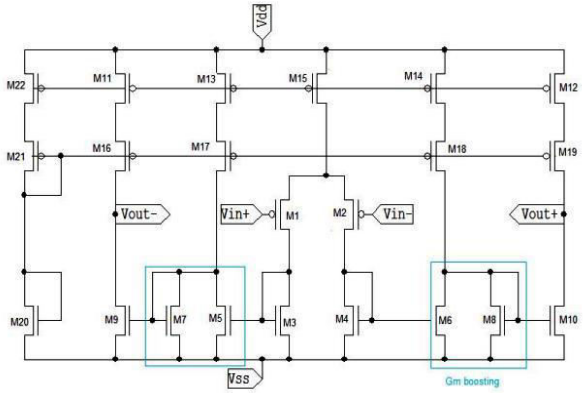

Figure.7 LNA circuit diagram

Figure7 shows the fully differential LNA circuit. Two sub-threshold PMOS input transistor pair M1 and M2 plays a vital role to reduce the flicker (1/f) noise in the circuit, because it cannot be eliminated in the succeeding stages[10]. Most of the designers prefer PMOS than NMOS; the reason behind this is NMOS gives more gain and more noise. To reduce the flicker noise, we have to choose the transconductance gm1 >> gm3 > gm5 by changing W/L ratio. To increase the transconductance of the input transistor, we use gm-boosting method to steer the current into the modified active load. The transconductance can be varied by changing the W/L ratio of the M5, M7. The above said condition also applicable to the negative counterpart of the amplifier.This proposed method of active load increases the gain of the amplifier with low power consumption. The transistors M20, M21and M22 provide the biasing to LNA.

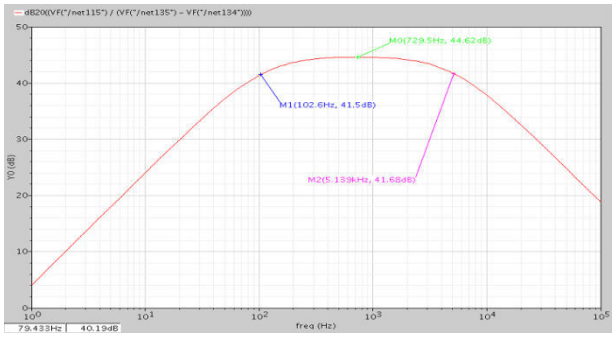

Figure 8. Gain Plot of LNA amplifier

VI. LNA NOISE ANALYSIS

Channel thermal noise of a MOSFET is derived from the noise current equation.

$$i_{n^2} = 4.\gamma.k.T.g_m \qquad (3)$$

Where, k – Boltzmann Constant; T – Absolute Temperature; g_m = transconductance.

The factor γ is a complex function of the basic transistor parameters and bias conditions. For modern CMOS processes with oxide thickness in the order of 50nm and with a lower substrate doping Nb of about 10^{15} – 10^{16} cm^{-3}, the factor $\gamma$is between 0.67 and 1[9].

$$v_{n,input}^2 = \frac{8\,kT\gamma}{g_{m1}}\left[1 + 2.\frac{g_{m10}}{g_{m1}}\frac{g_{m6}}{g_{m8}} + \frac{g_{m12}}{g_{m1}}\right] \qquad (4)$$

Therefore, to reduce input-referred thermal noise, the W/L ratios of M1&M2 and the lengths of M1 & M2 are chosen to be very large, thereby maximizing the transconductance of M1 & M2, while minimizing those of M9 and M10. The input devices are the primary source f flicker noise; therefore large area PMOS transistors are used.

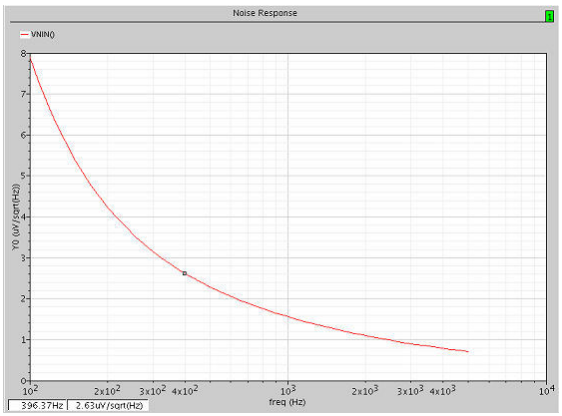

Figure 9. Input referred Noise Response

VII. LOW PASS FILTER

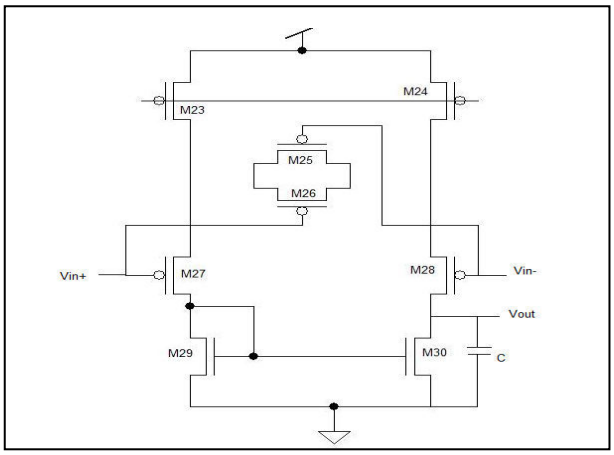

Figure 10 . High Linear Low Pass Filter.

High linear, OTA-C filter based simple Low pass filter is shown in the figure10. Linearity of the low pass filter is improved by source degeneration topology. In this circuit the transistors biased on triode region. M25-M26 work in a saturation-active mode for positive Vin in an active-saturation mode for negative Vin, Can result in a linear operation. The linear range is limited to V_{in}< V_{Dsat}.

The transconductance value for this low pass filter can be calculated from the equation given below.

$$g_m \approx \frac{g_{m27}}{1+\beta_{29}/4\beta_{23}} \qquad (5)$$

VIII. THE BULK DRIVEN SIGNAL PROCESSOR

For implantable bio-medical applications, gate-driven MOSFET posing threshold voltage constraint. A new processor using bulk-driven MOSFET has been developed to handle very small signals in the range of several millivolts. Both, bulk-driven and gate-driven performances are same except the physical size of former is small. The first order equation shows the V_{BS} and its effect on drain current.

$$i_D = K\left(V_{GS} - V_T - \frac{\eta}{2}V_{DS}\right)\cdot V_{DS} \quad \text{.....} V_{DS} \leq V_{DS.sat}$$

$$i_D = K(V_{GS} - V_T)^2 \cdot (1 + \lambda . V_{DS}) \quad \text{.....} V_{DS} \geq V_{DS,\,sat}$$

$$\text{Where, } \eta = 1 + \frac{\gamma}{2\sqrt{\varphi_j - V_{BS}}} \quad ; \quad V_{DS,sat} = \frac{V_{GS}-V_T}{\eta}$$

$$V_T = V_{TO} - \gamma\sqrt{2\phi_F - V_{BS}} + \gamma\sqrt{2\phi_F}$$

The seizure onset from the neural signal can be clipped-off by the processor. Later, it compared with the reference signal using high speed latch comparator. Thereby, seizure onset can be detected.

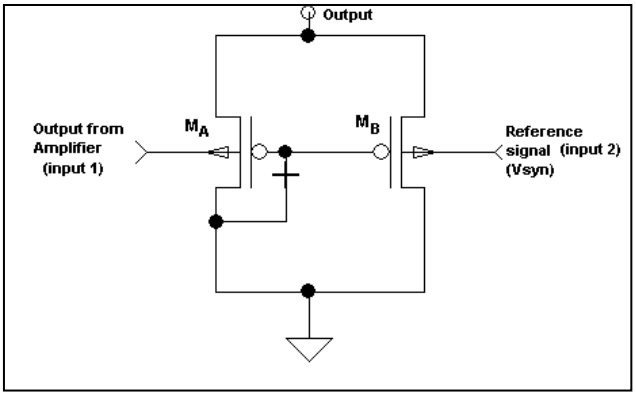

Figure11. A new Signal processing unit

The circuit used to extract the seizure onset is shown in the figure11. Neural signal from the amplifier is applied at the bulk of transistor M_A. Here, Gate and source is tied to make V_{GS} constant. Therefore, the output variation is only due to bulk potential. When input is greater than zero, inverse depletion layer is formed and it causes current to flow through the transistor M_A. The neural reference potential V_{SYN} for the normal behaviour is applied to the bulk of M_B.

The Combination of M_A& M_B blocks all signal whose value is less than the reference potential(V_{SYN}). Therefore the onset feature can be extracted.

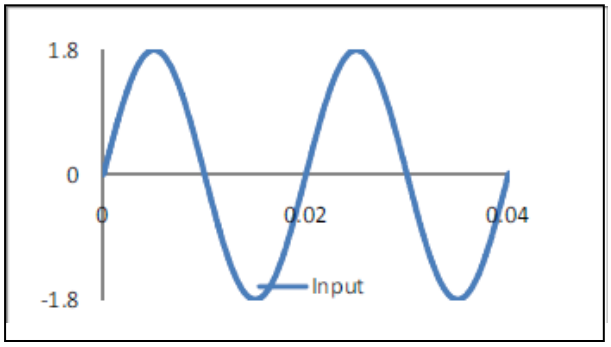

Figure 11.(a) Sample Input waveform

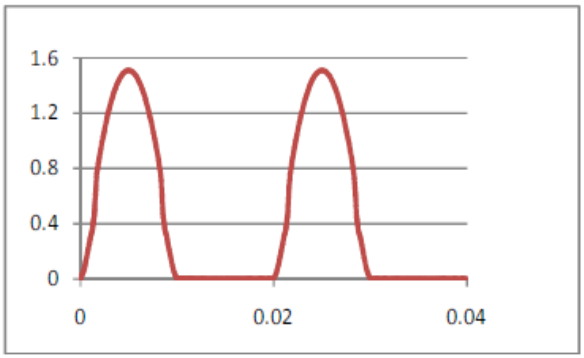

Figure 11.(b) Output waveform when Vsyn = 0 V

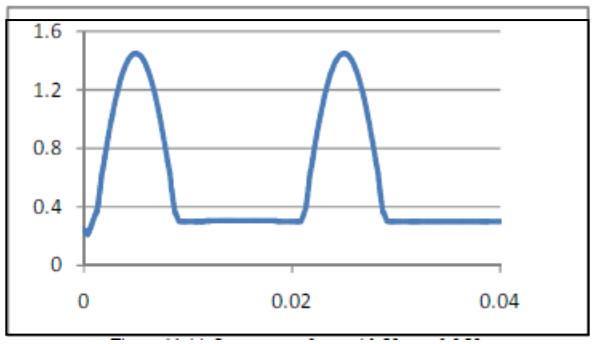

Figure 11.(c) Output waveform with Vsyn =0.3 V

TABLE 1: DEVICE SIZING

Device Sizing			
Length of all transistors = 0.18µm			
Devices	***Width (µm)***	***Devices***	***Width (µm)***
M1, M2	10	M20	0.24
M3,M4	2	M21,M22,M23	2
M5,M6	8	M24,M27,M28	2
M7,M8,M9,M10	2	M29,M30	0.5
M11,M12,M13	2	For Pseudo resistors	5
M14,M15,M16	2		
M17,M18,M19	2		

TABLE 2: SIMULATED PARAMETERS

S.No.	**Specification**	**Values**
1	Over-all Gain	44.6 dB
2	LFHPF cut-off Frequency	100Hz
3	LPF Cut-off frequency	5 KHz
4	CMRR	68dB
5	Input referred Noise	1.24 µV/sqrt(Hz)
6	Power Consumption	18.74 µw
7	Supply voltage	± 0.8 V

IX. CONCLUSION

The neural signal acquisition amplifier with 18.24µw and 1.24µVrms over the 100Hz – 5 KHz has been presented.A new signal processing circuit has been developed using 2 transistor reduces overall power consumption. Simulation results shows that this circuit is designed to meet all requirements for the detection and forewarning to the epilepsy affected patients for safety and clinical contexts.

ACKNOWLEDGEMENT

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Dynamic Voltage Restorer

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Abstract - Power quality is one of major concerns in the present era. It becomes important especially with the introduction of sophisticated devices, whose performance is very sensitive to the quality of power supply. Power quality problem is an occurrence manifested as a nonstandard voltage, current or frequency that results in a failure of end use equipments. One of the major problems dealt here is the power sag and swell.

To solve this problem, custom power devices are used. One of those devices is the Dynamic Voltage Restorer (DVR), which is the most efficient and effective modern custom power device used in power distribution networks. Its appeal includes lower cost, smaller size, and its fast dynamic response to the disturbance. This paper presents modeling, analysis and simulation of a Dynamic Voltage Restorer (DVR) using MATLAB. In this model a PI controller and Discrete PWM pulse generator was used in the control system.

Keywords *: DVR, voltage sag, swells, power quality, VSC.*

I. INTRODUCTION

Power quality is becoming an increasingly important topic in theperformance of many industrial applications such as information technology,significant influence on high technology devices related to communication, advancedcontrol, automation, precise manufacturing technique and on-line service.Users need constant sine wave shape, constant frequency and symmetricalvoltage with a constant root mean square (rms) value to continue the production. Tosatisfy these demands, the disturbances must be eliminated from the system. Thetypical power quality disturbances are voltage sags, voltage swells, interruptions,phase shifts, harmonics and transients [1][2].Among the disturbances voltage sag is considered the most severe since thesensitive loads are very susceptible to temporary changes in the voltage. Voltage sagis a short-duration reduction in voltage magnitude. The voltage temporarily drops to alower value and comes back again after approximately 150ms. Despitetheir short duration, such events can cause serious problems for a wide range of equipment [1][3].

The characterization of voltage sags is related with:

1. The magnitude of remaining voltage during sag
2. Duration of sag

In practice the magnitude of the remaining voltage has more influence than the duration of sags on the system. Voltage sags are generally within 40% of the nominal voltage in industry. Voltage sags can cost millions of dollars in damaged product, lost production, restarting expenses and danger of breakdown [2][3]. Short circuit faults, motor starting and transformer energizing will cause short duration increase in current and this will cause voltage sags on the line.

For certain end users of sensitive equipment the voltage correction devicemay be the only cost-effective option available.

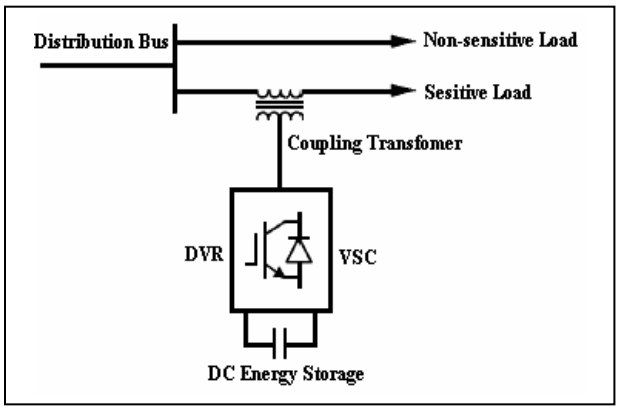


Figure.1: Basic Configuration of DVR

Different approaches exist to limit the costs caused by voltage dips and oneinteresting approach considered here is to use voltage source converters connected in series between the supply system and the sensitive load, this type of devices are often termed a Dynamic Voltage Restorer (DVR). Unlike uninterruptible powersupply (UPS), the DVR is specifically designed for large loads ranging from a few MVA up to 50 MVA or higher [8]. The DVR is fast, flexible and efficient solution to voltage sag problems. It can restore the load voltage within a few milliseconds and hence avoiding any power disruption to that load. The main idea of the DVR is detecting the voltage sag and injecting the missing voltage in series to the bus by using an injection transformer as shown in Figure 1.

The DVR can be divided into four component blocks, namely :

1.Voltage source PWM inverter

2. Injection/coupling transformer

3. Energy storage device

4. Filter unit.

II. PROPERTIOUS CHOICE OF DVR

There are numerous reasons why DVR is preferred over other devices [5]:

1. Although, SVC predominates the DVR but the latter is still preferred because the SVC has no ability to control active power flow.
2. DVR is less expensive compared to the UPS.
3. UPS also needs high level of maintenance because it has problem of battery leak and have to be replace as often as five years.
4. DVR has a relatively higher energy capacity and costs less compared to SMES device.
5. DVR is smaller in size and costs less compared to DSTATCOM
6. DVR is power efficient device compared to the UPS.

III. WORKING OF DVR

In the event of a fault on the load side of the DVR, DVR starts to generate the equivalent missing voltage and inject it to the line. DVR will continue the injection process until the bus voltage reaches its pre-fault value. DVR will inject three single-phase ac voltages with controllable amplitude and phase. The voltage sags resulting from faults can be corrected either in the transmission or distribution system shown in Fig.2. DVR can compensate small disturbances by injecting reactive power and compensate larger disturbances by injecting real power to the system.

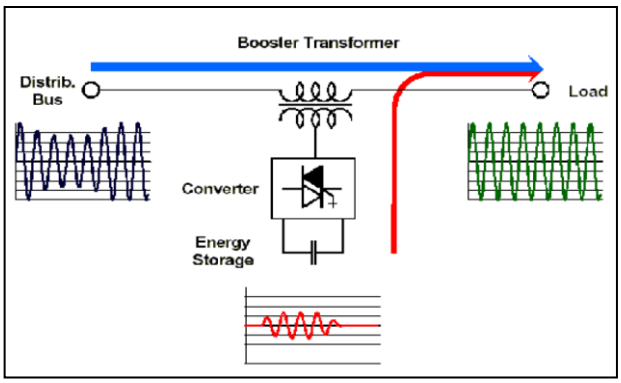


Figure.2: Working of DVR [2]

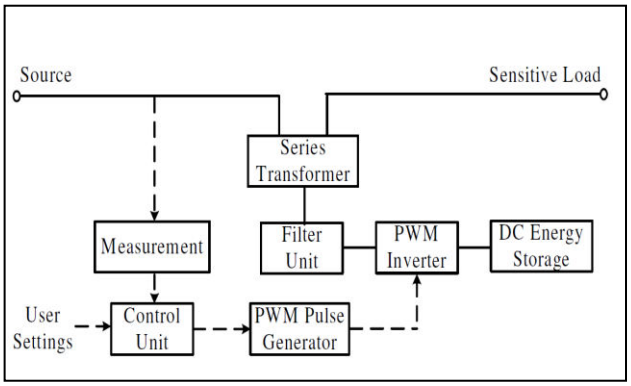


Figure.3: Simplified DVR block [3]

To obtain missing voltage DVR compares the distorted source voltage with its pre-fault value and then generate the control signal for PWM. The control unit gives information on required voltage to be inserted and its duration during sag. Sinusoidal pulse width modulation technique is used to control DVR. Solid-state power electronic switching devices are used in PWM. The output of PWM may contain harmonics and they can be filtered on the inverter side or the line side to smooth the voltage waveform. The filtering scheme should keep the total harmonic distortion (THD) of the remaining voltage at the supply side and the injected voltage within limits determined by standards as shown in Fig.3.

Voltage restoration of DVR needs to inject energy from DVR to distributionsystem. The required energy for injection during sag may be supplied from the grid or energy storage devices such as batteries or super conducting magnetic energy storage systems. However, the capability of energy storage that usually consists of capacitors in DVR is limited. Therefore, it must be considered how the injection energy can be minimized

during voltage sags and the load voltage can be made close to pre-fault voltage. This strategy is known as dynamic voltage restorer with minimum energy injection.

IV. CONVENTIONAL CONTROL STRTEGIES

Several control techniques have been proposed for voltage sag compensation such as pre-sag method, in-phase method and minimal energy control [2] [3] [7].

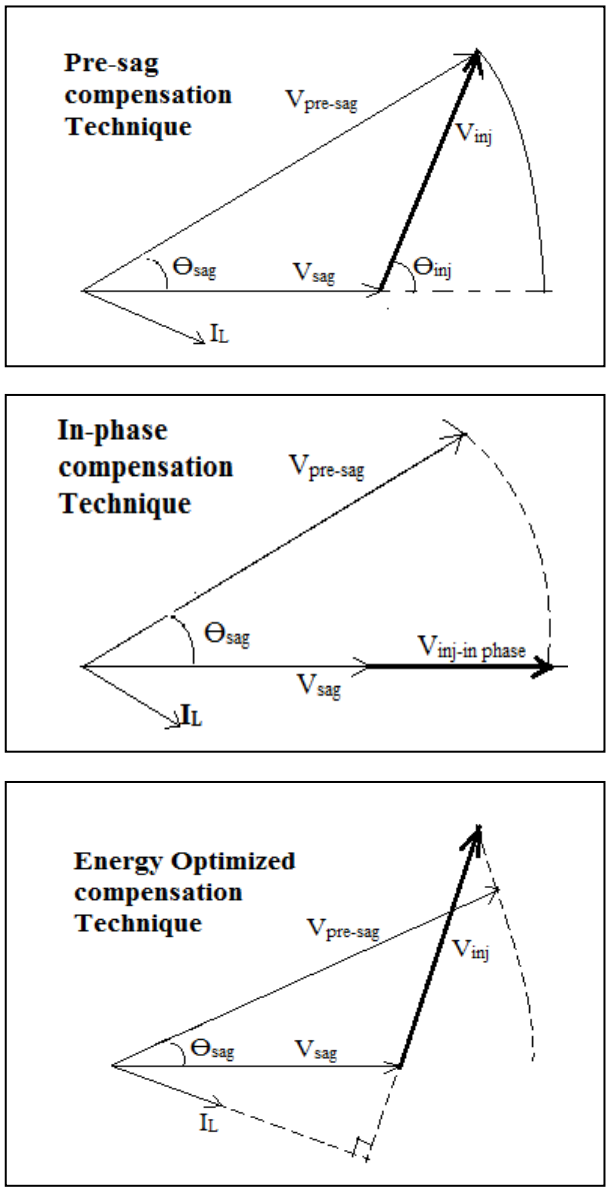


Figure.4: Conventional Control Strtegies if DVR [3] [7]

1. Pre-Sag Compensation Technique

The main defect of this technique is it requires a higher capacity energy storage device. Fig.4 shows the phasor diagram for the pre-sag control strategyin this diagram; Vpre-sag and Vsag are voltage at the point of common coupling (PCC), respectively before and during the sag. In this case VDVR is the voltage injected by the DVR, which can be obtained as:

Vpre-sag=VL, Vsag=Vs VDVR=Vinj

$$\text{Vinj} = \text{Vpre-sag} - \text{Vsag} \quad \ldots\ldots (1)$$

$$\theta\text{inj}=\tan^{-1}\{\frac{Vpre-sag\sin(\theta pre-sag)}{Vpre-sag\cos(\theta pre-sag)-Vsag\cos(\theta sag)}\} \quad \ldots\ldots (2)$$

2. In-Phase Compensation Technique

In this technique, only the voltage magnitude is compensated. VDVR is in-phase with the left hand side voltage of DVR. This method minimizes the voltage injected by the DVR, unlike in the pre-sag compensation. Fig.4 shows phase diagram for the in-phase compensation technique.

VDVR=Vinj

| Vinj | = | Vpre-sag |–| Vsag |

$$\angle Vinj = \theta inj = \theta s \qquad (3)$$

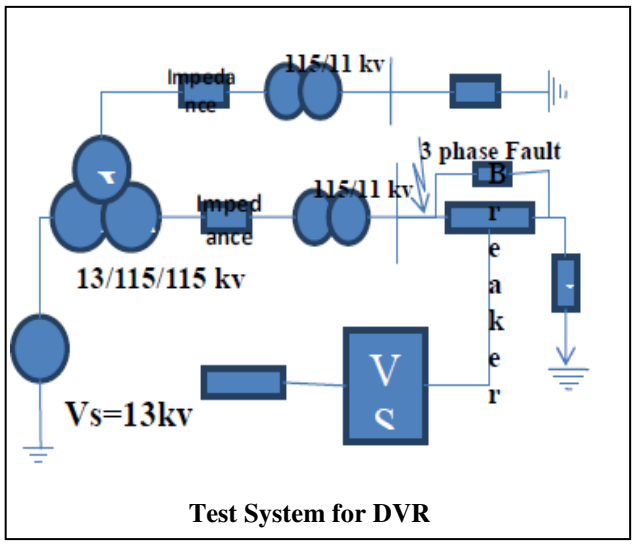
3. Energy Optimized compensation Technique

Pre-sag compensation and in-phase compensation must inject active power to loads almost all the time. Due to the limit of energy storage capacity of DC link, the DVR restoration time and performance are confined in these methods. The fundamental idea of energy optimization method is to make injection active power zero. In order to minimize the use of real power the voltages are injected at 90° phase angle to the supply current. Fig.4 shows a phasor diagram to describe the Energy optimization Control method.

The selection of one of these strategies influences the design of the parameters of DVR. In this paper, the control strategy adopted is Pre-sag compensation to maintain load voltage to pre fault value [7].

V. TEST SYSTEM FOR DVR

Single line diagram of the test system shown in the figure.5 for DVR is composed by a 13 kV, 50 Hz generation system, feeding two transmission lines through a 3- winding transformer connected in Y/S/S, 13/115/115 kV. Such transmission lines feed two distribution networks through two transformers connected in S/Y, 115/11 kV [6].



Test System for DVR

Figure.5 Single line diagram of the test system for DVR [3]

The DVR is simulated to be in operation only for the duration of the fault simulation model in MATLAB is shown in Fig.6.

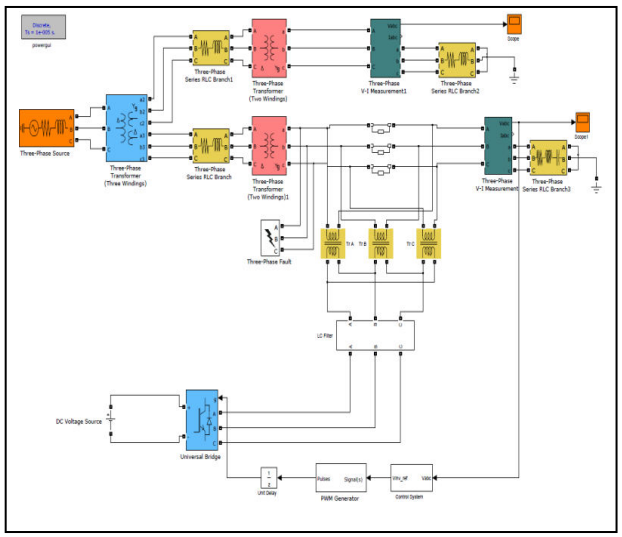


Figure.6 MATLAB mathematical model for the Test system

VI. SIMULATION RESULTS

Simulation is carried out in Matlab and fron that we are getting the result as following for differnts types of voltage sag and swell faults. from the result we can see that dynamiv voltage restorer restores the voltage when thw fault occurs.

In each of the following figure first result shows the intrupted voltage, second result shows the injected voltage and third figure shows the restored voltege.

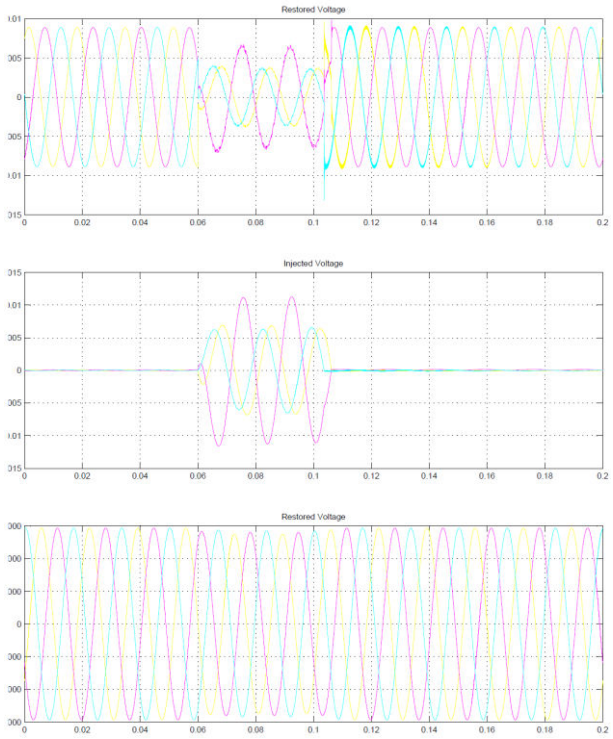


Figure.7 Single line to ground Sag Control

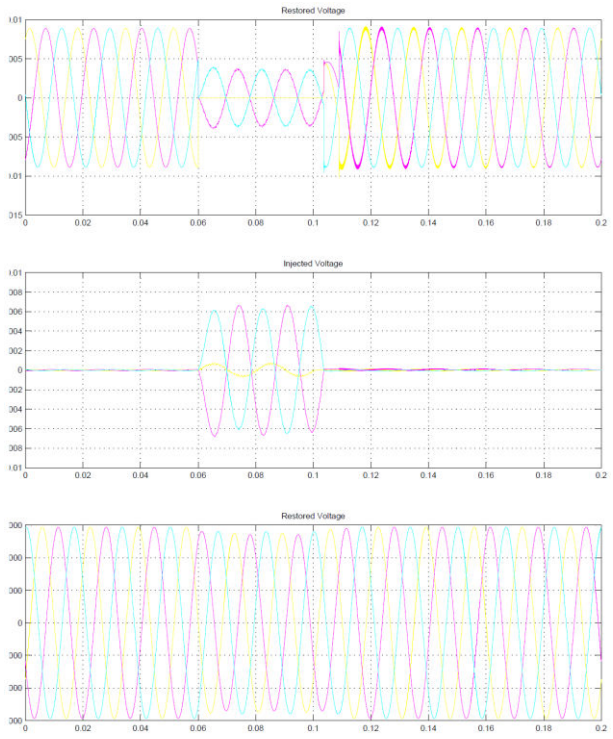


Figure.8 Two phase to ground Sag Control

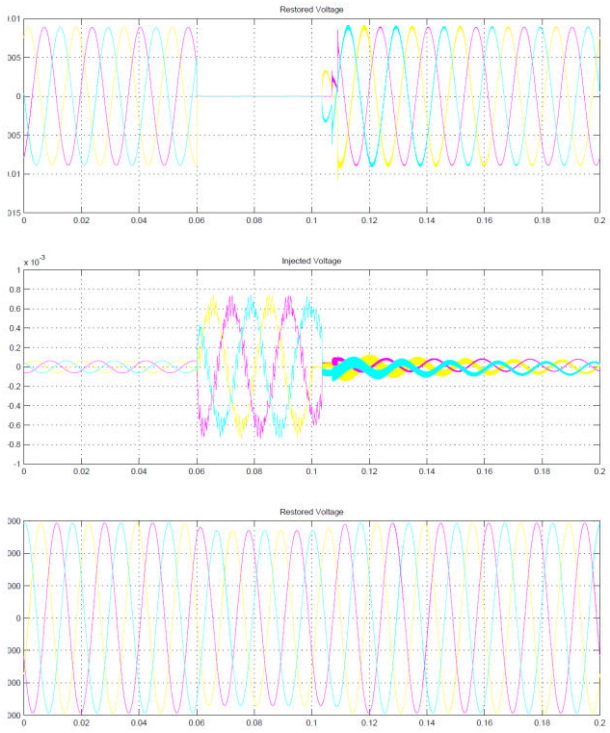


Figure.9 Three phase to ground Sag Control

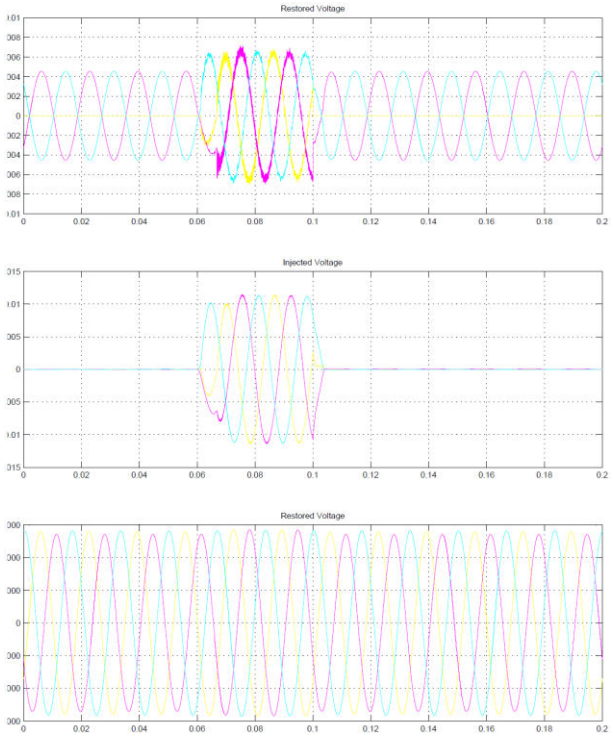


Figure.11 Double line to ground Swell Control

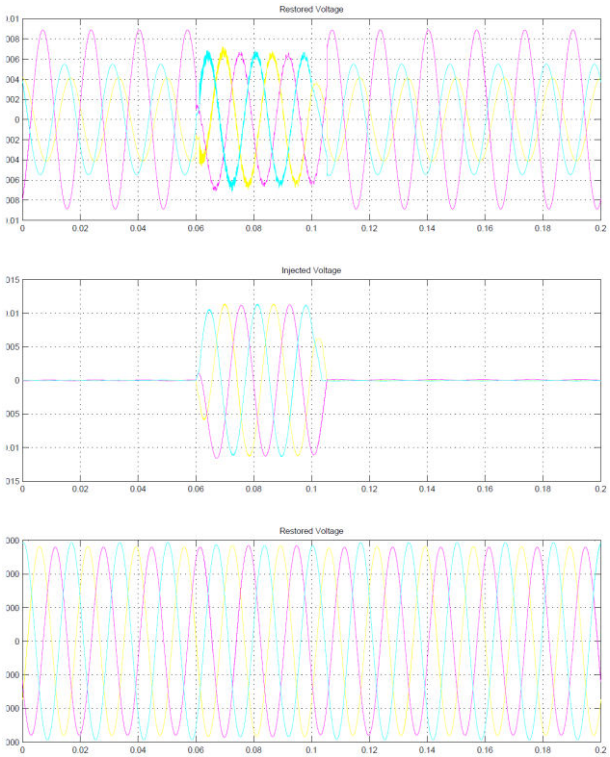


Figure.10 Single line to ground Swell Control

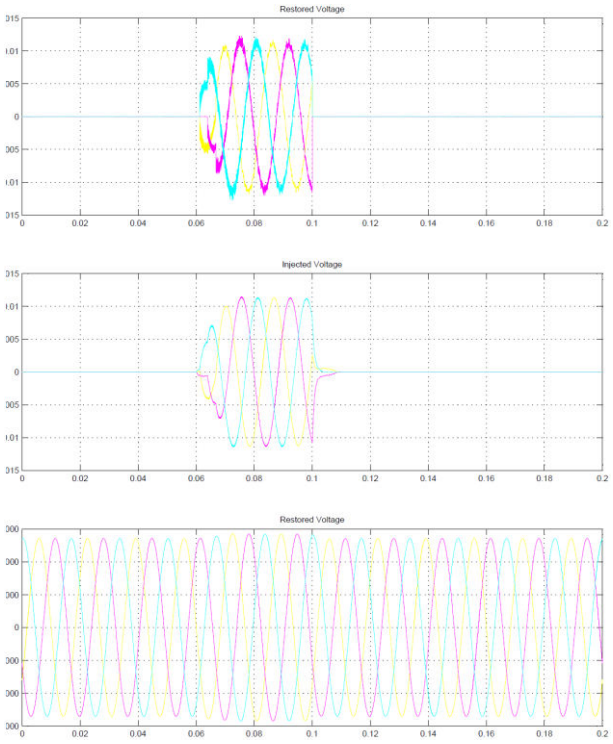


Figure.12 Three phase to ground Swell Control

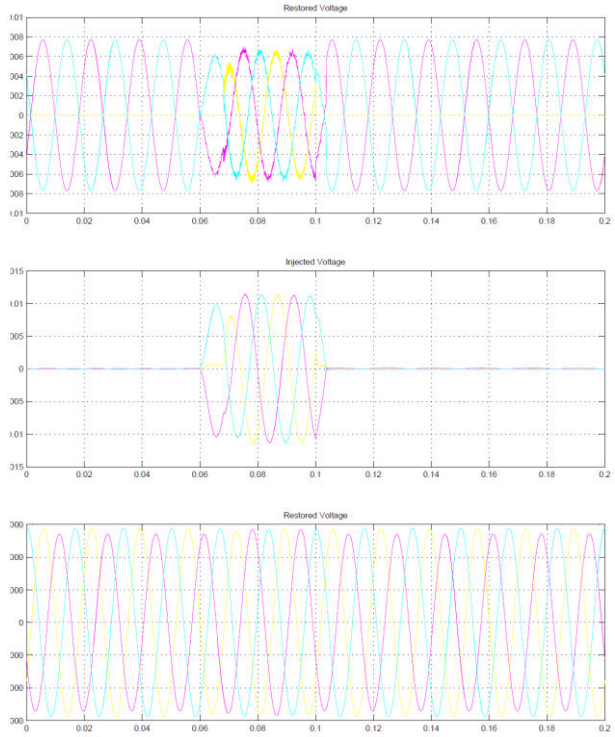


Figure.12 Line- line to ground Swell Control

VII. CONCLUSIONS

This paper has presented the power quality problems such as voltage dips, swells. Compensation techniques of custom power electronic devices DVR was presented. The design and applications of DVR for voltage sags andswells comprehensive results were presented. A PWM-based control scheme was implemented. As opposed to fundamental frequency switching schemes already available in the MATLAB/SIMULINK, this PWM control scheme only requires voltage measurements. This characteristic makes it ideally suitable for low-voltage custom power applications.

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High Speed CMOS Parallel Counter Design Based On State Decoding Logic

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Abstract— **Two different types high-speed parallel 8-bit counter architectures are proposed based on a novel approach for high speed counter design. The proposed parallel counter architectures consist of two sections – The *Counting Section* and the *State Decoding Module*. The counting section consists of three counting modules in which the first module (basic module) generates future states for the two remaining counting modules. The *State Decoding Module* decodes the count states of the basic module and carries this decoding over clock cycles through pipelined DFF to trigger the subsequent counting modules. The existing 8-bit parallel counter architecture consumed a total transistor count of 442 whereas the proposed parallel counters consumed only 274 transistors. The power dissipation of the existing parallel counter architecture and the proposed parallel counter architecture were 4.21mW(P_{INT}) and 3.60mW(P_{INT}) respectively at 250MHz. The worst case delay observed for the 8-bit counter using existing parallel counter architecture and the proposed parallel counter architectures were 7.481ns, 6.737ns and 6.677ns respectively using Altera Quartus II. A reduction in area(transistor count) by 38% and a reduction in power dissipation by 17.80% is achieved for the proposed counter architectures. The delay has been reduced by 0. 1% and 0.107% respectively for proposed methods I & II. Compared to the conventional 8-bit synchronous counter using JK flipflops a reduction in delay by 22.10% and 22.79% is achieved respectively for proposed high speed parallel counter methods I & II**

Index Terms—**Counter, divide-by-N, frequency divider, high speed, low-power, modules, modulus**

I. INTRODUCTION

HIGH SPEED COUNTER circuit is a fundamental need in most of the arithmetic applications. Basic properties preferred for a high speed counter includes high count rate , read on the fly and implementation suitable for VLSI.Counters are important building blocks in many fast arithmetic applications such as frequency division, shifting operation etc. Frequency dividers are basic blocks in numerous number of applications, such as generation of clock pulses of desired frequency, synchronization, data recovery and frequency synthesis in satellite communication systems. The counter blocks are designed with low power consumption, high speed and less area requirement for a particular application.

In order to reduce high counter power consumption, Alioto *et al.* [3] presented a low power counter design with a relatively high operating frequency. Alioto's design was based on cascading an analog block such that each counting stage's input frequency was halved compared to the previous counting stage . However, Alioto's counter design's carry chain rippled through all counting stages, resulting in a total critical path delay equal to the sum of all counting stage delays. Subsequently, Alioto's design was not well suited for large counter widths because the carry chain limited operating frequency even though the carry chain voltage was not rail-to-rail. S. Abdel-Hafeez *et al.* [2] proposed a simple implementation of frequency divider. However, the circuit had some design constraints to incorporate multiple frequency select inputs. A dual-modulus prescaler constructed with two parts-a synchronous counter and an asynchronous counter was proposed by B.Chang *et al.* [4].But the advantage of reduction in power consumption was negated by reduction in speed. Though it was a dual modulus divider, it won't provide the option of selecting two modulus values externally. As a substitution to the carry chain ,Kakarountas *et al.* [6] used a carry look-ahead circuit [5]. With the expense of an extra detector, the carry look-ahead circuit used a prescaler technique with systolic 4-bit counter modules using T-type flip-flops. The detector circuit output is used to enable counting in the higher order bits. Kakarountas's design used DFFs between the counter modules to improvise the operating frequency. As the counter design was limited by control signal broadcasting, Kakarountas's design was not practical for large counter widths.

The counting path of the 8-bit Parallel counting architecture [1] consists of four 2-bit modules separated by DFFs. Though the performance of the counter was found to be attractive, it consumed comparatively higher number of transistors thereby increasing total area required for the circuit realization. Therefore to negate these drawbacks of the counter architecture[1] alternative counter design strategies are proposed here. In the proposed architecture all the counting blocks are designed by using JK flipflops which reduces the number of gates required for its implementation. Also in place for repeating counting blocks of equal width, the counting blocks of variable width is used to reduce the size of the state decoding module.

Therefore two innovative digital CMOS parallel counter architectures are proposed here. Both the architectures used only JK flip flops for the counter design which reduces the design complexity. The remainder of the paper is organized as follows. Section II discusses about the proposed high speed parallel counter architectures. Section III provides a detailed discussion of the results and finally the conclusion is given in section IV.

II. The Proposed 8Bit Parallel Counter Architectures

The major advantages of the proposed parallel counter architectures are listed below.

1) All the individual blocks in the counting section are designed by using JK flipflops which reduces the number of gates required for its implementation of the circuit. Therefore, the transistor count of the counting path is reduced.
2) In place for repeating counting blocks of equal width, the counting blocks of variable width is used to reduce the size of the state decoding module. This also reduces the transistor count and thereby the area required for the realization of the counter.
3) The proposed counter has an operating frequency that is almost independent of counter width as a single clock input triggers all counting modules simultaneously.
4) The counter output is in radix-2 representation so read on-the-fly of the count value is possible with no additional logic decoding.
5) For higher counter width the proposed parallel counter architecture offers the advantage of reusability of modules and thus reduces the design time.

Method I:

Fig. 1 shows the functional block diagram of the proposed high speed parallel counter using method I. It consists of two sections – The *Counting section* and *State Decoding Module.*

1.Counting Section:

The counting section consists of four different modules. They are M_{13}, DFF_{PS}, and two subsequent counting modules (M_{2KS}). In the counting path the counting modules are separated by the pipelining flipflops DFF_{PS}.

i)Module- M_{13}

The basic module M_{13} is a parallel synchronous 3-bit up counter using JK flipflops. The schematic is shown in Fig.2. Here the J and K inputs of all the flip flops are shorted and thus its operation is equivalent to a T flipflop. The logic expressions of the outputs of the basic module M_{13} are given by,

$$Q_{00}(t+1) = J_0 Q'_{00}(t) + K'_0 Q_{00}(t) \quad (1)$$

$$Q_{01}(t+1) = Q_{00}(t)Q'_{01}(t)) + Q'_{00}(t)Q_{01}(t) \quad (2)$$

$$Q_{02}(t+1) = Q_{01}(t)Q_{00}(t)Q'_{02}(t)+[Q_{01}(t)Q_{00}(t)]'Q_{02}(t) \quad (3)$$

$$EN_1 = Q_{02}\, Q_{01}\, Q'_{00} \quad (4)$$

Here it has to be noted that $Q'_{00}(t)$ represents the complement of $Q_{00}(t)$. Q_{02} ,Q_{01} and Q_{00} represents the output bits of the basic module.

The first three equations can be simplified as,

$$Q_{00}(t+1) = 1 \text{ xor } Q_{00}(t) \quad (5)$$

$$Q_{01}(t+1) = Q_{00}(t) \text{ xor } Q_{01}(t) \quad (6)$$

$$Q_{02}(t+1)=[Q_{01}(t)Q_{00}(t)] \text{ xor } Q_{02}(t) \quad (7)$$

The module M_{13} is responsible for low-order bit counting and these three LSBs generate future states for all remaining modules in the counting path . In the counting path the enable output signal of module M_{13} is pipelined through flipflop DFF_{P1} to enable the counting operation of the first subsequent counting module. Whenever the module M_{13} output $Q_{02}Q_{01}Q_{00}$ =110 ,the input ST of the first subsequent counting module will be ' 1' after a single clock pulse. The counting module will change its state only if ST='1'. The connection between the basic and first subsequent counting module is such that when the basic module completes its full state sequence only, a single state change occurs for the first subsequent counting module.

i i)Module- M_{2KS}

The counting modules other than the basic module are represented here as M_{2KS}, where K represents the counter width of the counting module and S represents the position of the counting module after the basic module. The M_{2KS} counting module will change its state only if ST='1'. The two M_{2KS} modules shown in fig.3 are modules M_{221} and M_{232} respectively. Here module M_{221} is a two bit counting module and module M_{232} is a three bit counting module .

Fig.3 depicts the schematic diagram of module M_{221} and the output expressions are given by

$$Q_{10}(t+1)= ST \text{ xor } Q_{10}(t) \quad (8)$$

$$Q_{11}(t+1)= [ST\, Q_{10}(t)] \text{ xor } Q_{11}(t) \quad (9)$$

$$EN_{21}= Q_{11}\, Q_{10} \quad (10)$$

Where, Q_{11} and Q_{10} represents the output bits of the first subsequent module.

Fig.4 depicts the schematic diagram of Module- M_{232} of the proposed high speed parallel counter(Method I) and the output expressions are given by

$$Q_{20}(t+1)= ST \text{ xor } Q_{20}(t) \quad (11)$$

$$Q_{21}(t+1)= [STQ_{20}(t)] \text{ xor } Q_{21}(t) \quad (12)$$

$$Q_{22}(t+1)= [STQ_{21}(t)Q_{20}(t)] \text{ xor } Q_{22}(t) \quad (13)$$

$$EN_{22}= Q_{22}Q_{21}\, Q_{20} \quad (14)$$

Where, Q_{22}, Q_{21} and Q_{20} represent the output bits of the second subsequent module.

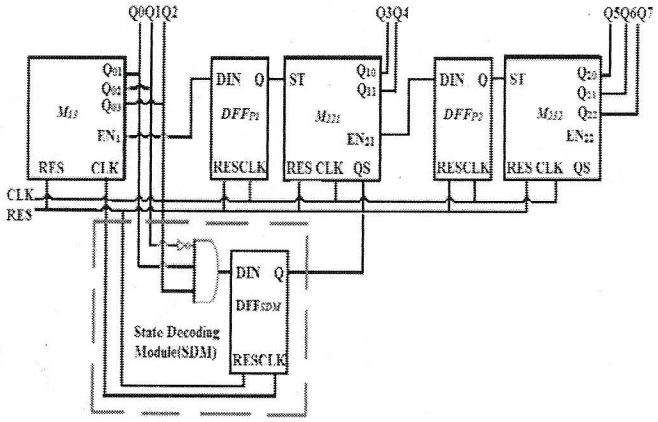

Fig. 1. Functional block diagram of the proposed high speed parallel counter

State Decoding Module (SDM):

The State Decoding module consists of a D flipflop DFF_{SDM}, a three input AND gate and an inverter. It decodes the count states of module M_{13}. This decoding is carried over two clock cycles through two DFFs(DFF_{SDM} of SDM and the second pipelining flipflop DFF_{P2} of the counting path) to trigger the second subsequent module M_{232}. In fig. 1, the counting path's first D flipflop(DFF_{P1}) decodes the low-order state $Q_{02}Q_{01}Q_{00}$ =110 and carries this decoding across one clock cycle and enables $Q_{11}Q_{10}$ =01 at module M_{221} on the next rising clock edge. The State Decoding module decodes the low-order state $Q_{02}Q_{01}Q_{00}$ ==101 and carries this decoding over two cycles. By Combining the one cycle mechanism in the counting path for $Q_{11}Q_{10}$ =10 and a two-cycle mechanism for $Q_{02}Q_{01}Q_{00}$ =101, $Q_{22}Q_{21}Q_{20}$ can be enabled. Thus all modules to be triggered concurrently on the clock edge, thus avoiding any rippling or long frequency delay. Fig. 5 shows the measured waveforms of the High Speed Counter using Altera Quartus II simulator at 250MHz.

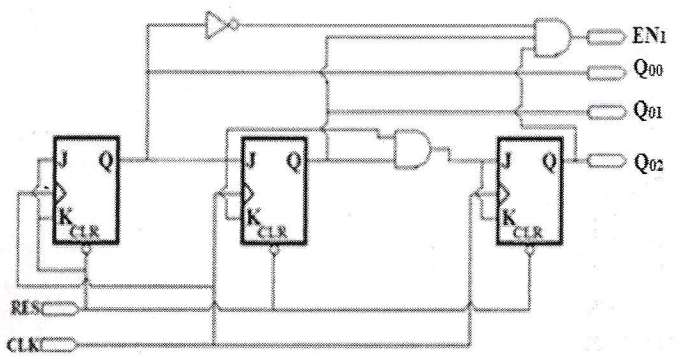

Fig. 2. The Schematic diagram of Module- M_{13} of the proposed high speed parallel counter(Method I)

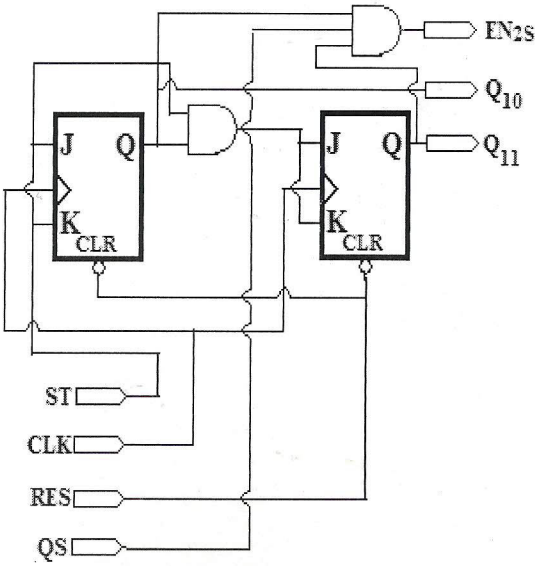

Fig. 3. The Schematic diagram of Module- M_{221} of the proposed high speed parallel counter(Method I)

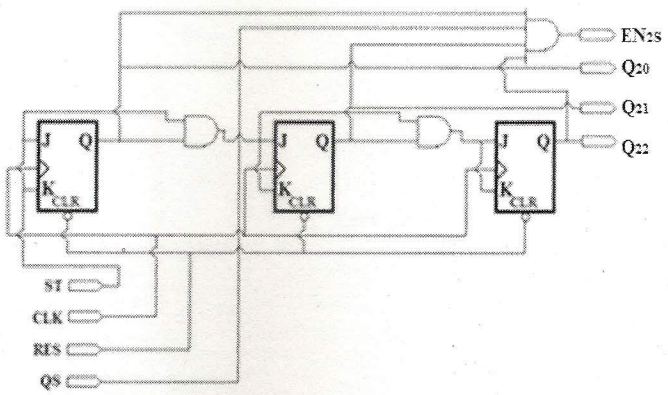

Fig. 4. The Schematic diagram of Module- M_{232} of the proposed high speed parallel counter(Method I)

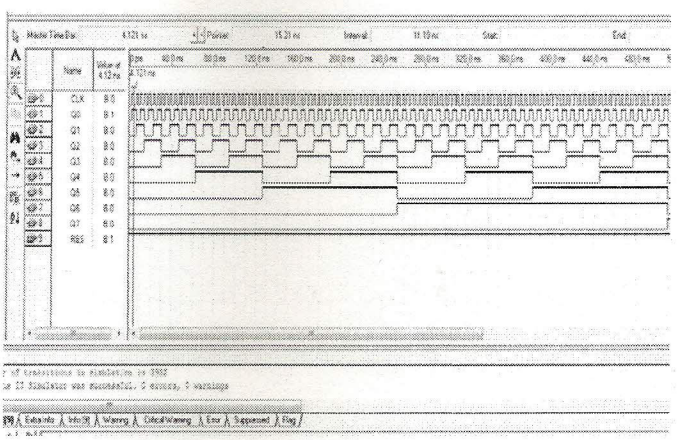

Fig.5. Measured waveforms of the proposed High Speed Counter using Altera Quartus II simulator at 250MHz

Method II:

Fig. 6 shows the functional block diagram of the proposed high speed parallel counter using method II. Similar to the parallel counter in fig. 1, it consists of two sections – The *Counting section* and *State Decoding Module.*

1.Counting Section:

The counting section consists of three different modules. They are M_{13}, DFF_{PS}, and two subsequent counting modules (M_{2KS}). Similar to method I, here also the counting modules are separated by the pipelining flipflops DFF_{PS} in the counting path.

i)Module- M_{13}

The basic module M_{13} is a parallel synchronous 2-bit up counter using JK flipflops. The schematic is shown in Fig.7. Here the J and K inputs of the flip flops are shorted and thus its operation is equivalent to a T flipflop. The logic expressions of the outputs of the basic module M_{13} are given by,

$$Q_{00}(t+1) = J_0Q'_{00}(t) + K'_0Q_{00}(t) \quad (15)$$

$$Q_{01}(t+1) = Q_{00}(t)Q'_{01}(t)) + Q'_{00}(t)Q_{01}(t) \quad (16)$$

$$EN_1 = Q_{01}\,Q'_{00} \quad (17)$$

The equations (15) and (16) can be simplified as,

$$Q_{00}(t+1) = 1 \text{ xor } Q_{00}(t) \quad (18)$$

$$Q_{01}(t+1) = Q_{00}(t) \text{ xor } Q_{01}(t) \quad (19)$$

The module M_{13} is responsible for low-order bit counting and these two LSBs generate future states for all remaining modules in the counting path. In the counting path the enable output signal of module M_{13} is pipelined through flipflop DFF_{P1} to enable the counting operation of the first subsequent counting module. Whenever the module M_{13} output $Q_{01}Q_{00}$ =10 ,the input ST of the first subsequent counting module will be ' 1' after a single clock pulse. The counting module will change its state only if ST='1'. The connection between the basic and first subsequent counting module is such that when the basic module completes its full state sequence only, a single state change occurs for the first subsequent counting module.

i i)Module- M_{2KS}

Fig.8 depicts the schematic diagram of module M_{2KS}. The two M_{2KS} modules shown in fig.8 are modules M_{231} and M_{232} respectively.

The output expressions of module M_{231} are given by,

$$Q_{10}(t+1) = ST \text{ xor } Q_{10}(t) \quad (20)$$

$$Q_{11}(t+1) = [ST\,Q_{10}(t)] \text{ xor } Q_{11}(t) \quad (21)$$

$$Q_{12}(t+1) = [STQ_{11}(t)\,Q_{10}(t)] \text{ xor } Q_{12}(t) \quad (22)$$

$$EN_{21} = Q_{12}Q_{11}\,Q_{10} \quad (23)$$

Similarly, the output expressions of module M_{232} are given by,

$$Q_{20}(t+1) = ST \text{ xor } Q_{20}(t) \quad (24)$$

$$Q_{21}(t+1) = [STQ_{20}(t]) \text{ xor } Q_{21}(t) \quad (25)$$

$$Q_{22}(t+1) = [STQ_{21}(t)\,Q_{20}(t)] \text{ xor } Q_{22}(t) \quad (26)$$

$$EN_{22} = Q_{22}Q_{21}\,Q_{20} \quad (27)$$

State Decoding Module (SDM):

The State Decoding module (SDM) consists of a D flipflop DFF_{SDM}, a two input AND gate and an inverter. It decodes the count states of module M_{13}. The State Decoding logic of the proposed high speed parallel counter of fig.6 decodes the count states of its basic module, M_{13}. This decoding is carried over two clock cycles through two DFFs(DFF_{SDM} of SDM and the second pipelining flipflop DFF_{P2} of the counting path) to trigger the second subsequent module M_{232}. In fig. 6, the counting path's first D flipflop(DFF_{P1}) decodes the low-order state $Q_{01}Q_{00}$ =10 and carries this decoding across one clock cycle and enables $Q_{12}Q_{11}Q_{10}$ =001 at module M_{231} on the next rising clock edge. The State Decoding logic decodes the low-order state $Q_{01}Q_{00}$ ==01 and carries this decoding over two cycles. By Combining the one cycle mechanism in the counting path for $Q_{12}Q_{11}Q_{10}$ =110 and a two-cycle mechanism for $Q_{01}Q_{00}$ =01, $Q_{22}Q_{21}Q_{20}$ can be enabled. Thus all modules to be triggered concurrently on the clock edge, thus avoiding any rippling or long frequency delay.

Fig. 9 shows the measured waveforms of the High Speed Counter using Altera Quartus II simulator at 250MHz.

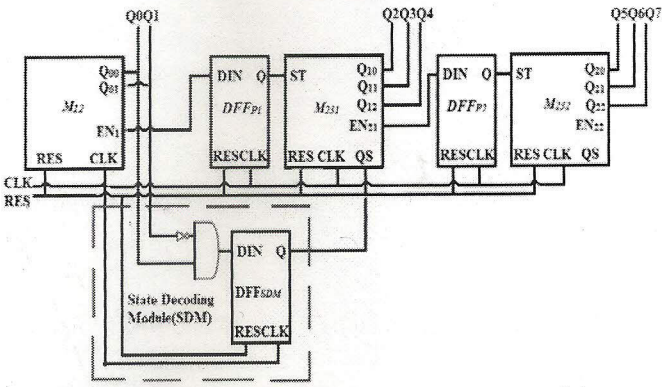

Fig. 6. Functional block diagram of the proposed high speed parallel counter

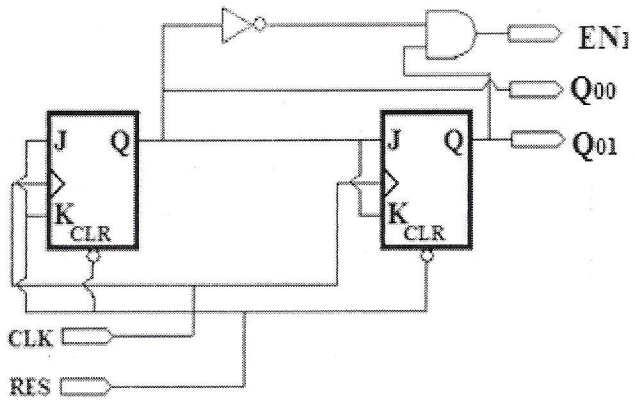

Fig. 7. The Schematic diagram of Module- M_{13} of the proposed high speed parallel counter(Method II)

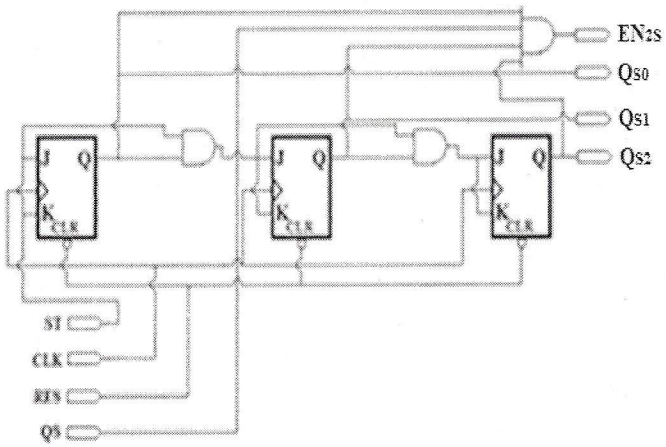

Fig. 8. The Schematic diagram of Module- M_{2KS} of the proposed high speed parallel counter(Method II)

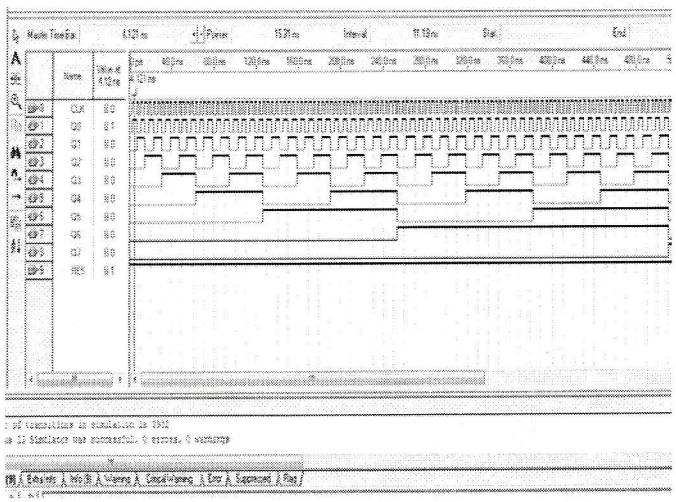

Fig. 9. Measured waveforms of the proposed High Speed counter(Method II) using Altera Quartus II simulator at 250MHz

III. Results And Discussions

In this section the performance of the proposed high-speed low power parallel 8-bit counter architectures are is analyzed and compared with the existing parallel counter architecture. Note that for all the observations the device cyclone EP1C20F400C7 is used here. The transistor count, power dissipation and delay of the high speed counter using existing technique is tabulated in Table I. The Power dissipation of the counter at 250 MHz was found to be 3.54 mW(P_{INT}) and the delay was 7.481ns. The measured values of the proposed high speed parallel counter(method I) using Altera Quartus II simulator are listed in Table II. The Power dissipation of the counter at 250 MHz was found to be 2.91mW(P_{INT}) and the delay was 7.737ns. The measured values of the proposed high speed parallel counter(method II) using Altera Quartus II simulator are listed in Table III. The Power dissipation of the counter at 250 MHz was found to be 2.91mW(P_{INT}) and the delay was 7.677ns.

TABLE I
PERFORMANCE ANALYSIS OF THE HIGH SPEED PARALLEL COUNTER(USING EXISTING METHOD)

Parameter	Transistor count	Delay (worst case)	Power Dissipation(P_{INT})
	442	7.481ns	3.54 mW

TABLE II
TRANSISTOR COUNT OF THE PROPOSED DUAL MODULUS DIGITAL CMOS FREQUENCY DIVIDER(USING PARALLEL COUNTER OF METHOD I)

Parameter	Transistor count	Delay (worst case)	Power Dissipation(P_{INT})
	274	6.737ns	2.91 mW

TABLE III
PERFORMANCE ANALYSIS OF THE PROPOSED HIGH SPEED PARALLEL COUNTER(METHOD II)

Parameter	Transistor count	Delay (worst case)	Power Dissipation(P_{INT})
	274	6.677ns	2.91 mW

Table IV shows that a reduction in area(transistor count) by 38% and a reduction in power dissipation by 17.80% is achieved for the proposed counter architectures compared to the existing work by S. Abdel-Hafeez *et al.* [1]. A reduction in delay by 0. 1% and 0.107% is achieved for proposed methods I & II respectively. When compared with existing Digital CMOS Parallel counter [1], the proposed Parallel counters show improved performance in terms of power consumed, delay and area. Compared to the conventional 8-bit synchronous counter using JK flipflops a reduction in delay by 22.10% and 22.79% is achieved respectively for proposed high speed parallel counter methods I & II.

TABLE IV

COMPARISON OF PERFORMANCE OF PARALLEL COUNTER ARCHITECTURES

Parameter	*Power P_{INT}(mw)*	*Delay(ns)*	*Power Delay Product(PDP) $X10^{-12}$ Joules*	*Area in transistor count*
Conventional 8-bit synchronous counter	2.30	8.648	19.89	196
8-bit parallel counter- S. Abdel-Hafeez et al.,[1]	3.54	7.481	26.48	442
The 8-bit parallel counter using proposed methodI	2.91	6.737	19.60	274
The 8-bit parallel counter using proposed methodII	2.91	6.677	19.43	274

IV. CONCLUSION

In this paper, performance of the proposed high-speed low power parallel 8-bit counter architectures are is analyzed and compared with the existing parallel counter architectures. The existing 8-bit parallel counter architecture consumed a total transistor count of 442 whereas the proposed parallel counters consumed only 274 transistors. The power dissipation of the existing parallel counter architecture and the proposed parallel counter architecture were 4.21mW(P_{INT}) and 3.60mW(P_{INT}) respectively at 250MHz. The worst case delay observed for the 8-bit counter using existing parallel counter architecture and the proposed parallel counter architectures were 7.481ns, 6.737ns and 6.677ns respectively using Altera Quartus II. A reduction in area(transistor count) by 38% and a reduction in power dissipation by 17.80% is achieved for the proposed counter architectures. The delay has been reduced by 0. 1% and 0.107% respectively for proposed methods I & II.

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TABLE IV

COMPARISON OF PERFORMANCE OF PARALLEL COUNTER ARCHITECTURES

Parameter	*Power P_{INT}(mw)*	*Delay(ns)*	*Power Delay Product(PDP) $X10^{-12}$ Joules*	*Area in transistor count*
Conventional 8-bit synchronous counter	2.30	8.648	19.89	196
8-bit parallel counter- S. Abdel-Hafeez et al.,[1]	3.54	7.481	26.48	442
The 8-bit parallel counter using proposed methodI	2.91	6.737	19.60	274
The 8-bit parallel counter using proposed methodII	2.91	6.677	19.43	274

IV. CONCLUSION

In this paper, performance of the proposed high-speed low power parallel 8-bit counter architectures are is analyzed and compared with the existing parallel counter architectures. The existing 8-bit parallel counter architecture consumed a total transistor count of 442 whereas the proposed parallel counters consumed only 274 transistors. The power dissipation of the existing parallel counter architecture and the proposed parallel counter architecture were 4.21mW(P_{INT}) and 3.60mW(P_{INT}) respectively at 250MHz. The worst case delay observed for the 8-bit counter using existing parallel counter architecture and the proposed parallel counter architectures were 7.481ns, 6.737ns and 6.677ns respectively using Altera Quartus II. A reduction in area(transistor count) by 38% and a reduction in power dissipation by 17.80% is achieved for the proposed counter architectures. The delay has been reduced by 0. 1% and 0.107% respectively for proposed methods I & II.

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Implementation of Scalable Encryption Algorithm Using Reversible Logic

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***Abstract*—Scalable Encryption Algorithm is widely used in embedded system for security purpose where power consumption is considered to be a critical problem. In addition, encryption system demands not only high security but low power consumption. Reversible logic are of interest for power minimization and are very much in demand for future computing as they are known to produce zero power dissipation under ideal conditions. This paper is about the design and implementation of Scalable Encryption algorithm using Reversible logic gates. By using a series of reversible gates, the design of reversible circuits for the functional modules of Scalable Encryption Algorithm has been realized.**

Keywords-Reversible Logic Gates, Scalable Encryption Algorithm, Low power Cryptography.

I. INTRODUCTION

Reducing power dissipation is considered to be one of the major goal in VLSI circuit design. R. Landauer in early 1960's demonstrated that computation carried using irreversible logic results in energy dissipation due to the information loss [1]. It is proved that loss of each bit of information dissipates atleast KTln2 joules of energy, where K = $1.3806505 \times 10^{-23} m^2 kg^{-2} k^{-1}$ (Joules $Kelvin^{-1}$) is the Boltzmann's constant and T is the absolute temperature at which the computation is performed [1]. In 1973, Bennet showed that zero power dissipation is possible [2] if the computation is carried out in a reversible way. Reversible computation in a system can be performed only when the system is comprised of reversible gates. Reversible logic operation do not lose information and has zero power dissipation under ideal conditions, since the amount of energy dissipated is directly proportion to the number of bits erased during computation.

Reversible logic has become promising area of study in recent years. The various research areas where reversible logic are intensively studied and applied are low power CMOS design, Optical computing, Quantum computing, Bioinformatics, DNA computing and Nanotechnology.

Scalable encryption algorithm plays a major role in providing security in controllers, smart cards, processors and small embedded applications. Encryption systems demands not only on high security but also on low power consumption. Reversible logic provides solution in low power design of embedded systems. In this paper, the functional blocks of Scalable Encryption Algorithm is designed and implemented using reversible logic gates.

II. REVERSIBLE GATES

A. Reversible Logic

An n-input n-output function is said to be reversible only if the input vector can be uniquely determined from the output vector and there is one to one mapping between inputs and outputs. Then the number of input and output lines are equal.

B. Reversible Logic Gates

A nxn reversible gate can be represented as:

$I_v = (I_1, I_2, I_3,..., I_n)$

$O_v = (O_1, O_2, O_3,....,O_n)$

where I_v and O_v are input and output vectors respectively. The following is an example of a reversible gate. Table 1.a represents the truth table for regular XOR gate. For the regular XOR, from the output X, the input A,B cannot be predicted as there is no one to one mapping between the inputs and outputs, where as from table 1(b), which is the truth table for reversible XOR gate, the input A,B can be predicted from output P,Q.

Table 1(a) Regular XOR

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

Table 1(b) Reversible XOR

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Synthesis of Reversible logic circuits is more complicated than conventional logic circuits, since no feedback and fan-out is allowed in reversible circuits [3]. A Reversible logic circuit should have the following features [4].

- Use minimum number of reversible gates.
- Use minimum number of garbage outputs.
- Use minimum constant inputs.

The output that is not used for further computation is called garbage outputs [5]. The constant input is the additional input added in the nxn function to make it reversible [6].

Several reversible logic gates have been proposed in the past years. Some of the popular reversible gates are: Feynman Gate (FG) [7], Toffoli Gate (TG) [8], Fredkin Gate (FRG) [9], Peres Gate (PG) [10], HNG gate [11].

The Feynman Gate, also known as controlled-not gate (1-CNOT) is a 2x2 reversible gate that can be described by the equations: P = A and Q =A⊕B, where 'A' is the controlled bit and 'B' is the data bit. Feynman Gate can be used as a copying gate. Since fan-out is not allowed in reversible logic, this gate is used for duplication of the required outputs. It is shown in Figure 2.

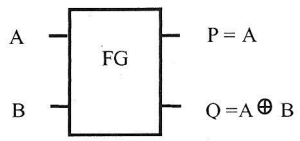

Figure 2 Feynman Gate

Toffoli Gate, also known as controlled controlled-not (CCNOT), is a 3x3 reversible logic gate. Toffoli Gate is a universal reversible logic gate, which means any reversible circuit can be constructed from Toffoli Gate. Toffoli Gate is as shown in Figure 3.

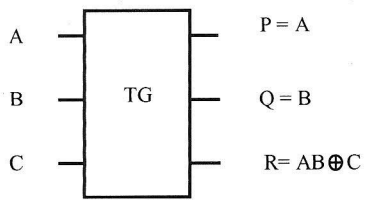

Figure 3 Toffoli gate

Figure 4 shows the 3x3 Fredkin Gate. Fredkin Gate is also known as controlled permutation gate.

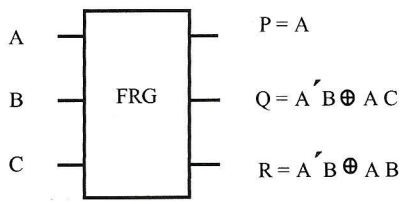

Figure 4 Fredkin gate

Peres Gate is a 3x3 reversible gate, also known as New Toffoli Gate (NTG). Peres Gate is equal with the transformation produced by a Toffoli Gate followed by a Feynman Gate. Peres Gate is as shown in Figure 5.

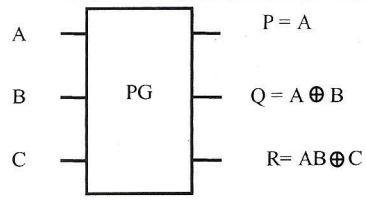

Figure 5 Peres Gate

HNG Gate is a 4x4 reversible logic gate. The HNG Gate is shown in Figure 6. One of the prominent function of HNG Gate is that it can work in single as a reversible full adder unit.

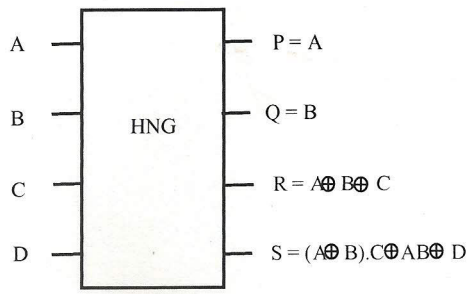

Figure 6 HNG gate

III. SCALABLE ENCRYPTION ALGORITHM

Scalable Encryption Algorithm is a parametric block cipher for resource constrained systems (e.g., sensor networks, RFIDs). It was initially designed as a low-cost encryption/authentication routine (i.e., with small code size and memory) targeted for processors with a limited instruction set (i.e., AND, OR, XOR gates, word rotation, and modular addition). Compared to older solutions for low-cost encryption like Tiny Encryption Algorithm (TEA), Yuval's proposed, Scalable Encryption Algorithm (SEA) benefits for a stronger security analysis, derived from recent advances in block cipher design/cryptanalysis. SEA has been proven to be an efficient solution for embedded software applications using microcontrollers.

A. Parameters and Definitions

$SEA_{n,b}$ operates on various text, key and word sizes. It is based on a Fiestel structure with variable number of rounds, and is defined with respect to the following parameters

- n plaintext size, key size;
- b processor (or word) size;
- nb = n/2b number of words per Fiestel branch;
- nr number of block cipher rounds.

As an only constraint, it is required that n is a multiple of 6b. Let x be a n/2-bit vector. The following representations are considered.

- Bit representation: x_b = x((n/2)-1.....x(1) x(0)).
- Word representation: $x_w = x_{nb-1}\, x_{nb-2}\, \ldots\ldots\, x_2\, x_1\, x_0$.

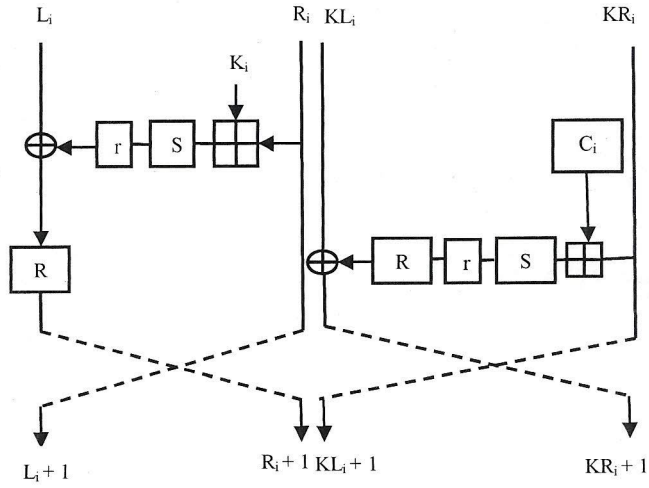

Figure 7 Encrypt/Decrypt round and key round

B. Basic Operations

Due to its simplicity constraints, $SEA_{n,b}$ is based on a limited number of elementary operations denoted as follows [12].

1. Bitwise XOR $\oplus$.
2. Addition mod 2^b
3. A 3-bit Substitution box, S = {0,5,6,7,4,3,1,2} that can be applied to any set of 3-bit words for efficiency purposes.
4. Word rotation R, defined on nb-word vectors:

$$R: x \rightarrow y = R(x) \leftrightarrow y_{i+1} = x_i \ , \ 0 <= i <= nb-2$$

$$y_0 = x_{nb-1}$$

5. Bit rotation r, defined on nb-word vectors

$$r: x \rightarrow y = r(x) \leftrightarrow \ y_{3i} = x_{3i} >>> 1$$

$$y_{3i+1} = x_{3i+1}$$

$$y_{3i+2} = x_{3i+2} <<< 1$$

Where $0 <= i <= (nb/3) - 1$ and >>> and <<< respectively, represents the cyclic right and left shifts inside a word.

The encrypt round F_E, decrypt round F_D, and key round F_k are pictured and defined as

$$[L_{i+1}, R_{i+1}] = F_E(L_i, R_i, K_i) \quad \leftrightarrow R_{i+1} = R(L_i) \oplus r(S(R_i \boxplus K_i))$$

$$L_{i+1} = R_i$$

$$[L_{i+1}, R_{i+1}] = F_D(L_i, R_i, K_i) \quad \leftrightarrow R_{i+1} = R^{-1}(L_i \oplus r(S(R_i \boxplus K_i)))$$

$$L\,i_{+1} = Ri\,[\,KL_{i+1}, KR_{i+1}\,]$$

$$[KL_{i+1}, KR_{i+1}] = F_K(KL_i, KR_i, C_i) \leftrightarrow KR_{i+1} = KL_i \oplus R(r(S(R_i \boxplus K_i)))$$

$$KL_{i+1} = KR_i$$

IV. REVERSIBLE LOGIC FUNCTIONAL MODULES FOR THE DESIGN OF SEA

The Scalable Encryption Algorithm has five functional blocks: Word rotate R, Inverse Word rotate R^{-1}, Bit rotate r, Bitwise XOR and Substitution box S. The Substitution box function is done by interchanging the bit positions.

A. Word rotate

The Word rotate function can be implemented using Barrel shifter. A barrel shifter is a digital circuit that can shift a data word by a specified number of bits in one clock cycle. It is constructed using sequence of 2 to 1 multiplexers. A reversible 2 to 1 MUX has been designed using one Fredkin Gate [13]. The equation for 2 to 1 MUX can be written as, $P = AS' \oplus BS$, where S is the select bit and A,B works as input. Figure 8 shows Fredkin Gate as reversible 2 to 1 MUX.

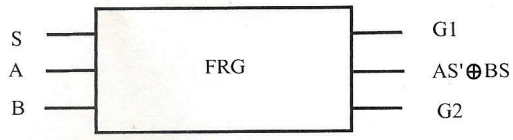

Figure 8 Fredkin Gate as reversible 2 to 1 MUX

B. Bit rotate

The bits inside the word are rotated using Shift Register, which is constructed using D-flip flop. The reversible form of D-flip flop has been designed using two Fredkin Gate and three Feynman Gate.

Feynman Gate is used as a copying gate, since fan-out is not allowed, this gate is useful for duplication of the required outputs. Figure 9 shows the reversible form of D-flip flop.

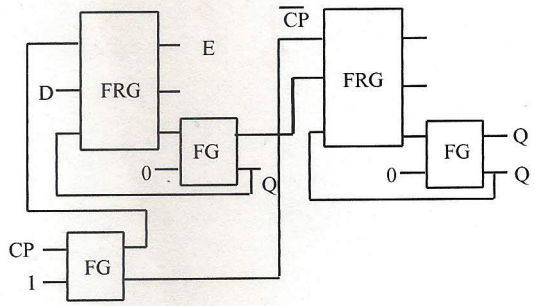

Figure 9 Reversible D-flip flop

The reversible Shift Register [14] constructed using reversible D-flip flop is as shown in Figure 10 .

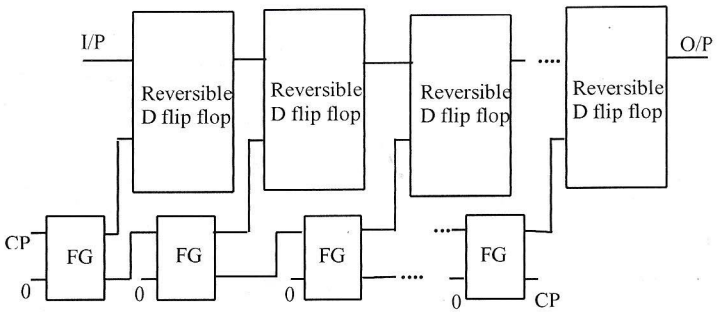

Figure 10 Reversible Shift Register

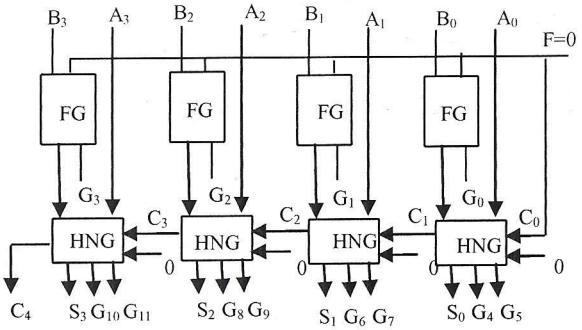

Figure 11 Reversible carry propagate adder

C. Mod 2^b addition

The optimized and efficient mod 2^b adder is designed using carry propagate adders [15].The design of reversible mod 2^b adder can be implemented using reversible carry propagate adder and it is constructed using Feynman Gate and HNG gate [11].

D. Bitwise XOR

Single Feynman Gate is used to perform reversible Bitwise XOR operation.

V. Reversible Design of SEA

The Figure 12 shows the 48-bit Encrypt/Decrypt round of SEA designed using Reversible logic.

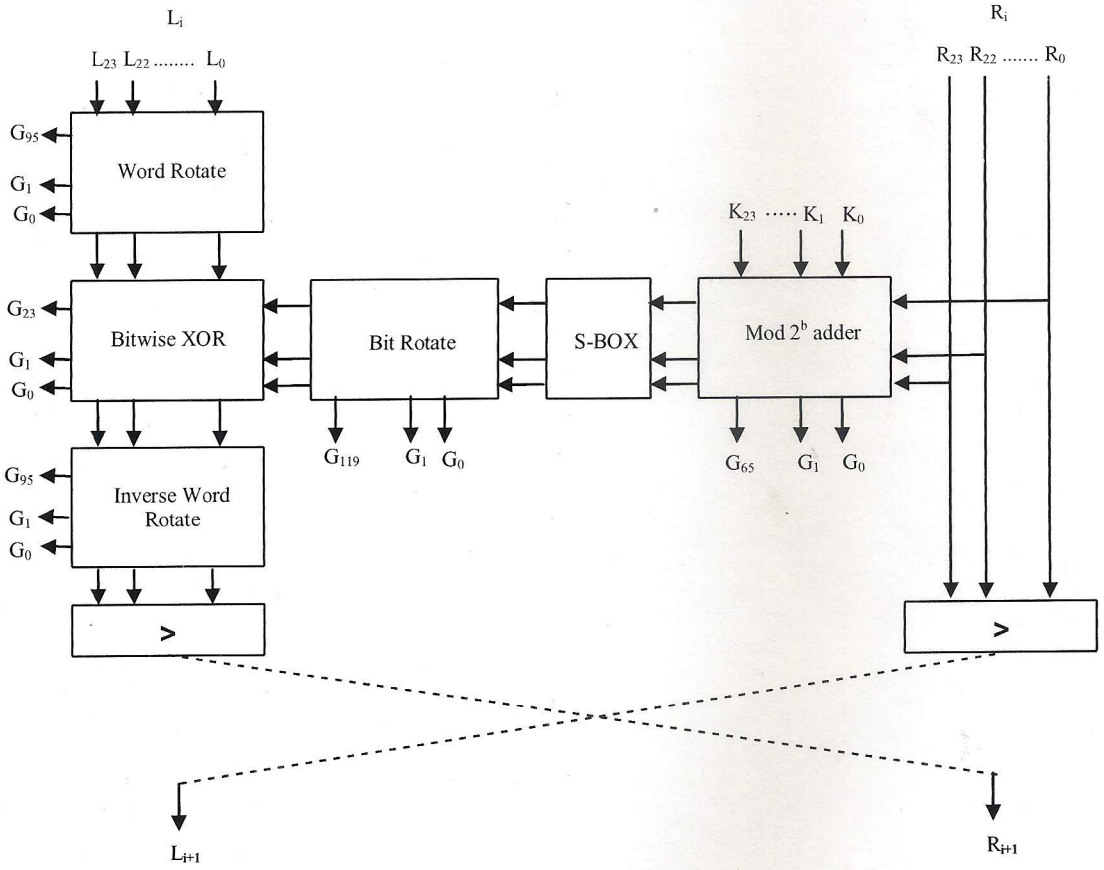

Figure 12 Reversible design of Encrypt/Decrypt round of Scalable Encryption Algorithm

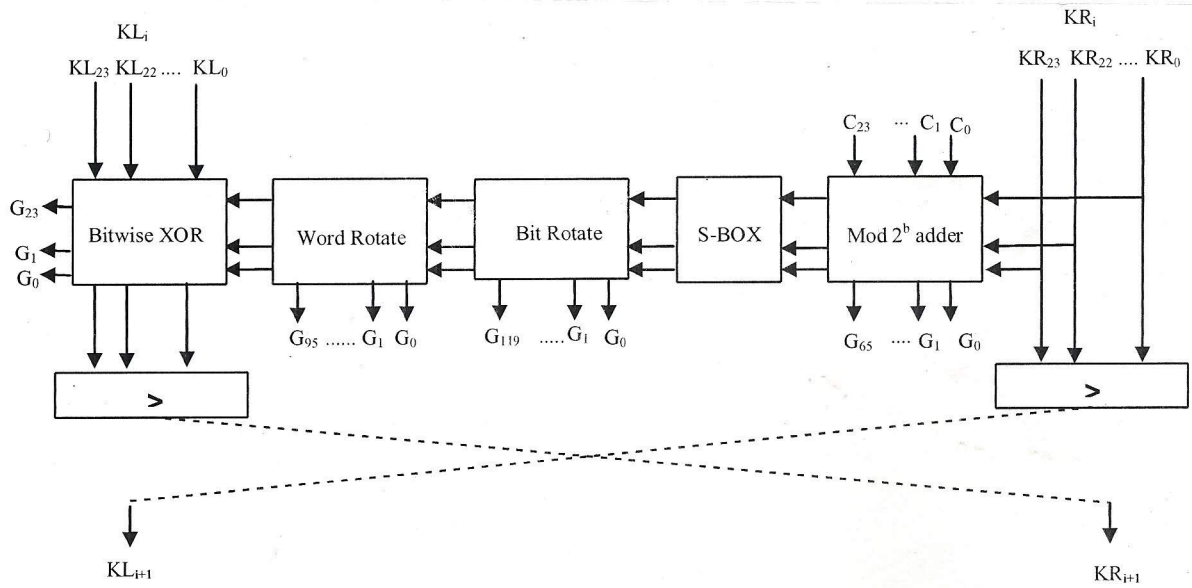

Figure23 Reversible design of Key round of Scalable Encryption Algorithm

The Figure 13 shows the Reversible key generation round of Scalable Encryption Algorithm.

VI. CONCLUSION AND FUTURE WORK

In this paper, the functional modules of Scalable Encryption Algorithm is analyzed and designed using Reversible logic gates. On this basis, the Encrypt/Decrypt round of SEA is designed using Reversible logic. Although in this process, the number of garbage outputs are increased, the designed system ensures consumption of very little heat since, reversible logic operations do not lose information.

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Performance Enhancement of Solar Photovoltaic System Using Fuzzy Logic Controller

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Abstract - Photovoltaic array exhibits non linear characteristics of power for varying insolation and temperature. So it is necessary to track the peak power in each power curves of the PV system to enhance the performance. Here in this paper a PV array is modeled using its mathematical equations and its peak power is extracted by using Fuzzy logic controller Technique. The proposed fuzzy logic controller is successful in tracking maximum power point of solar PV system and their simulation results are shown in this paper. The whole work is carried out in Simulink/MATLAB environment. This method is most efficient as the controller used for maximum power point tracking is fast when compared to other conventional algorithms (P&O .etc)

Keywords - *Maximum power point (MPP), maximum power point tracking, Fuzzy logic controller, boost converter.*

I. INTRODUCTION

World is much more concerned about the fossil fuel exhaustion, ecosystem damage and finally global heating nowadays. So we have to go for a clean, reliable and economic energy resource. Photovoltaic energy is coming under this category [1].By using photovoltaic energy we can avoid transmission losses and damaging ecosystems. Owing to the cheap availability of electrical energy from PV cells, they are extensively used in air conditioning water pumping in remote as well as urban areas. But unpredictable whether condition implies the characteristics of solar cells to be a non linear. Thus it requires a special design consideration to extract the available amount of energy at its maximum efficiency. Due to the ease of implementation and low cost and simplicity in design consideration, here in this paper we are opting Fuzzy logic controller for tracking maximum power point. Here, the temperature and irradiance is the parameters are taken into consideration. Depending on the parameters the I-V & P-V characteristics of PV array are simulated &presented in this paper.

II. MODELING OF PV ARRAY

The basic principle of photovoltaic cell is its ability to convert light energy to electrical energy [1]. PV cell is basically a p-n junction semiconductor. In dark, the solar cell exhibits the exponential characteristics as its output characteristics which are similar to diode characteristics. That is, when light energy falls on solar cell, the electrons will be excited from the current state of being attached to the atoms, because of increase in its energy greater than band gap energy. So electron-hole pairs will the created. Under the influence of internal electric fields of p-n junction, a current starts flowing through the closed the path [8]. This current is depending on the quanta of light energy incident on the PV array. Under the short circuit condition, current will be flowing through the external circuit. And when the external resistance is increased up to infinity which the condition is similar to the open circuit condition, the current doesn't flow. Thus the characteristics of PV cell depend on the loading effect.

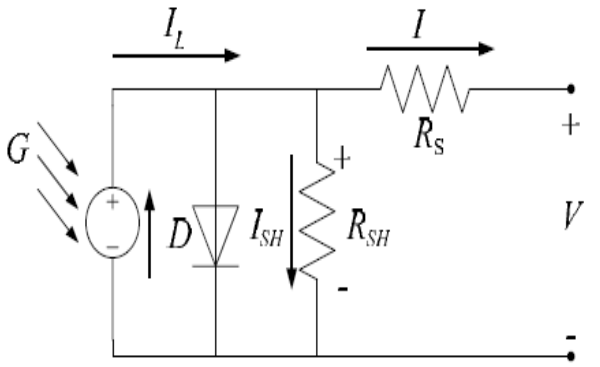


Fig. 1: Equivalent circuit of PV cell

When light is falling on PV array, a photocurrent I_L is produced. When then there is dark, PV cell acts as a diode. So there is no voltage and current at this time until if it is connected to an external supply. The diode or diode current will be produced only there is an external supply.

For better result such as precision, we are taking diode saturation current I_o, leakage resistance representing R_{sh}, internal resistance R_s and diode quality factor A. But in an ideal cell Rs and R_{sh} will be zero. So we can represent the solar cell in a mathematical equation as

$$I = I_l - I_o\left(e^{\frac{q(V+IRs)}{AkT}} - 1\right) \quad (1)$$

Where q is the electron charge q=1.6e-^{19} C and k is boltzmann's constant k=1.38e-^{23}J/K

Photocurrent I_l which depends on temperature can be written as

$$I_{l=}I_{L(T1)} + ko(T - T_1) \quad (2)$$

$$I_{L(T1)} = I_{sc(T1,nom)}\frac{G}{G_{(nom)}} \quad (3)$$

$$k_o = \frac{I_{sc(T2)} - I_{sc(T1)}}{(T_2 - T_1)} \quad (4)$$

$$I_{o(T1)} = \frac{I_{sc(T1)}}{e^{\frac{qV_{oc(T1)}}{nk_1}} - 1} \quad (5)$$

The internal resistance Rs can be represented by

$$R_s = \frac{dV}{dI_{voc}} - \frac{1}{X_v} \quad (6)$$

Where

$$X_v = I_{o(T1)}\frac{q}{nkT1}e^{\frac{qV_{oc(T1)}}{nkT1}} - \frac{1}{X_v} \quad (7)$$

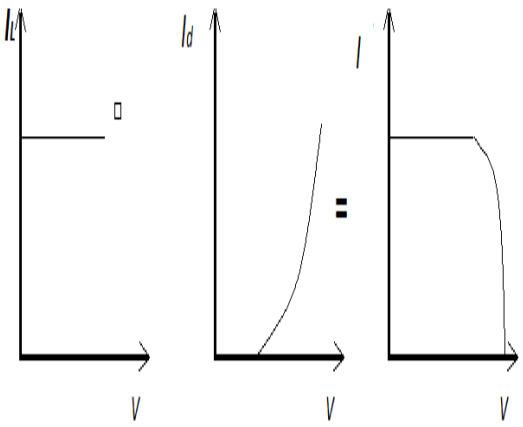


Fig. 2 : I-V characteristics of solar panel

III. PROPOSED CONTROL SYSTEM

The main control objective of this paper is to track the maximum power point of PV system for different solar irradiance using Fuzzy logic controller technique. This technique is more efficient because the proposed fuzzy logic controller technique is fast and efficient for values of solar radiations changing time to time when compared to conventional algorithms where abrupt tracking is not possible. The proposed block diagram of fuzzy logic controller technique is shown below.

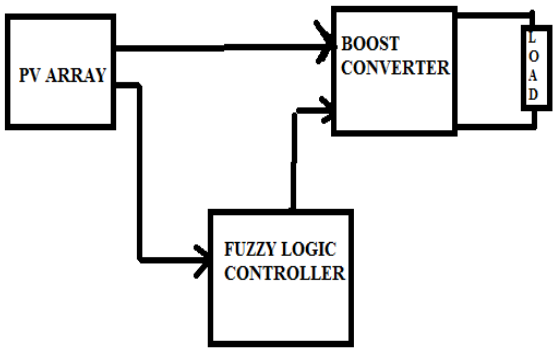


Fig. 3 : Proposed circuit diagram

IV. CONTROL STRUCTURE OF FUZZY LOGIC CONTROLLER (FLC)

The basic control structure of FLC is shown below, it mainly consists of two inputs as shown below i(p) and Δi(p) and outputs of FLC is U(k).The operation of FLC mainly takes place with the fuzzification of input values and control them by using rule basis functions and again defuzzifying it for further application

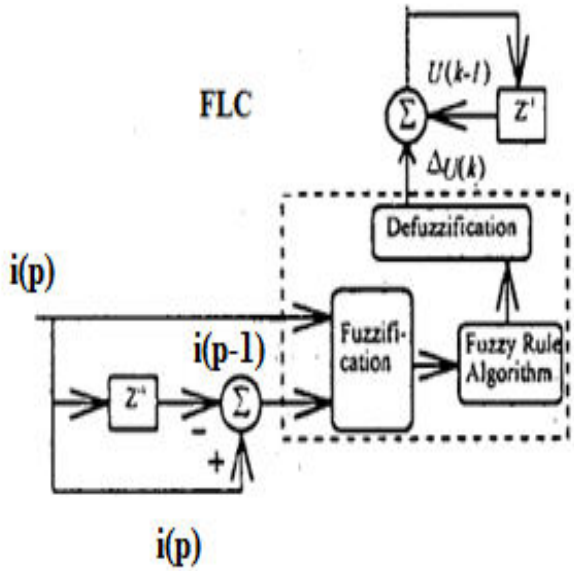
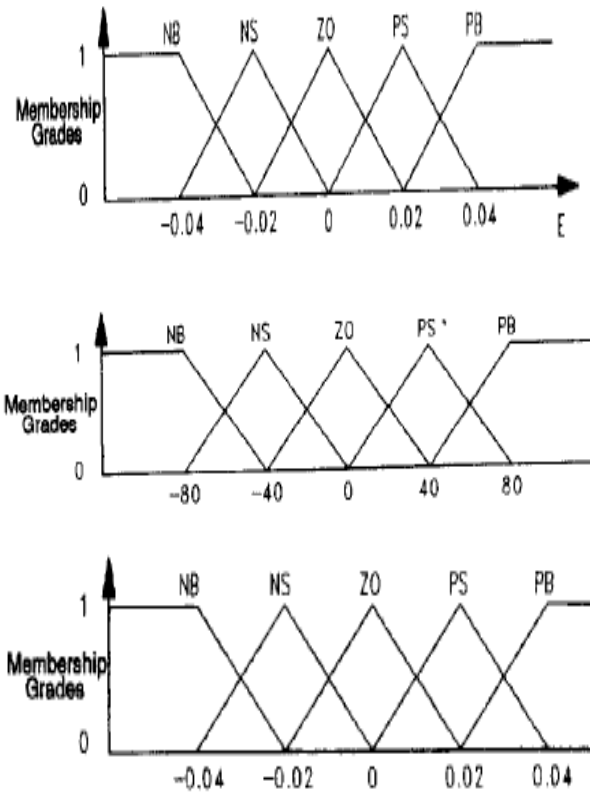


Fig. 4 : Basic diagram of fuzzy logic controller

A. Fuzzification

Fuzzy logic is an effective paradigm to handle imprecision. It can be used to take fuzzy or imprecise [1,2] observations for inputs and yet arrive at crisp and precise values for outputs .The process of fuzzification mainly deals with converting precise inputs to values which are imprecise or vague. i.e Fuzzification is the process of making a crisp quantity to fuzzy. In general the input variables are expressed as membership functions in terms of fuzzy labels such as PB (positive big), PS (positive small), ZO(zero), **NS** (negative small), **NB** (negative big) using basic fuzzy subset, there are many types of membership functions are used but in this paper triangular membership function is taken into consideration



The above shown are the figures for two inputs and one output membership function.

i. Rule basis function

In this rule basis function input are given in the form of fuzzy sets as shown in below table .The inputs i(p) and Δi(p) are converted into fuzzy sets and are formed in the form of rule basis

CE / E	NB	NS	ZE	PS	PB
NB	ZE	ZE	PB	PB	PB
NS	ZE	ZE	PS	PS	PS
ZE	PS	ZE	ZE	ZE	NS
PS	NS	NS	NS	ZE	ZE
PB	NB	NB	NB	ZE	ZE

Fig. 5 : Fuzzy rule viewer table

The rule table are generated such that the input must always be zero. In general rule base instruction which is used is given below

IF' i(p) is PB AND Δi(p) is ZO THEN dD is PA.

B. Defuzzification

The process of converting fuzzy sets to single crisp value is called defuzzification and the reverse process of it is fuzzification .Several methods are available for the process of defuzzification like centroid, centre of sums, mean of maxima ,among which centroid method is mostly commonly used defuzzification method.

$$P^* = \int \mu(p)\, p\, dp \,/\, \int \mu(p)\, dp \quad ....(i)$$

Where

μ(p) – Membership function

p – Elements

V. MAXIMUM POWER POINT TRACKING USING FUZZY LOGIC CONTROLLER

The maximum power point tracking of solar pv system mainly depends on factor such as insolation , temperature .

The fuzzy logic is efficient in tracking maximum power point because unlike other conventional mppt algorithms it don't want exact knowledge of solar characteristics

The input V(p) is the load point for which we have to achieve the maximum power point and here ΔV(P) is

the change in error this value is changed according to the load point it helps in the movement of load point in order to reach the maximum power point .The inference used in this paper is mamdani function.

$$\Delta I(p) = I(p) - I(p-1) \quad ...(ii)$$

$$\Delta V(p) = V(p) - V(P-1) \quad ...(iii)$$

PARAMETER	VALUE
Inductance L	1e-2 H
Capacitance C	1e-2 F
Switching frequency	1Khz

Table 1. parameters values used in simulation

VI. SIMULATION RESULTS

The experimental setup of MPPT using Fuzzy Logic Controller is simulated in MATLAB for different value of temperature and irradiation. The characteristics (P-V) of PV module is simulated using MATLAB which is shown below in fig.4

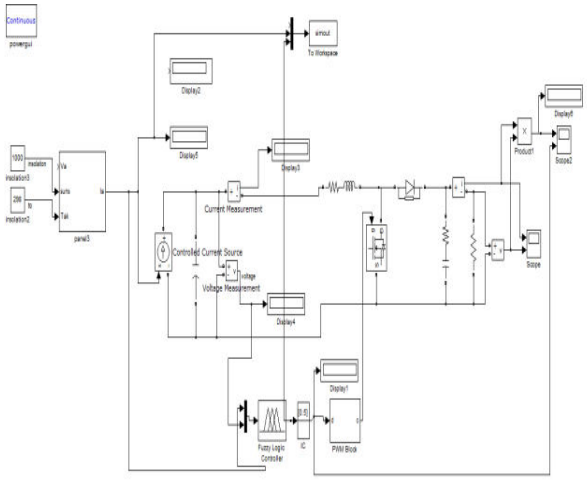


Fig. 6: Simulation diagram of MPPT using FLC algorithm

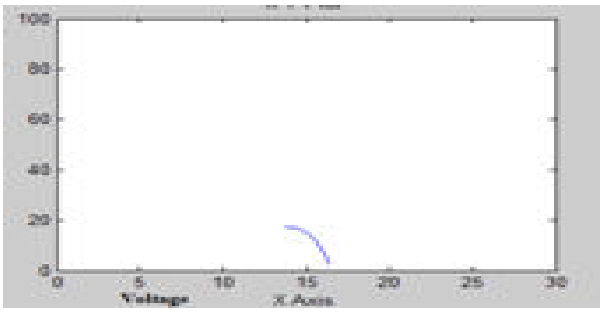


Fig. 7 : P-V characteristics of proposed simulation

The FIS file and the rule viewer used in proposed simulation setup for maximum power point tracking for solar pv system is shown below in fig .9, fig .10

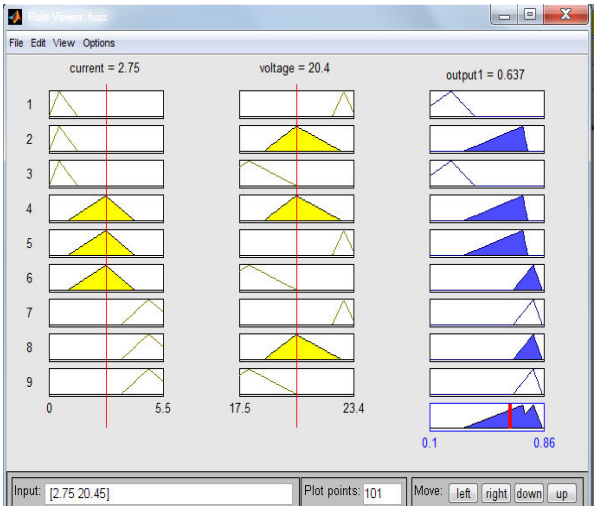


Fig. 8 : Fuzzy FIS table

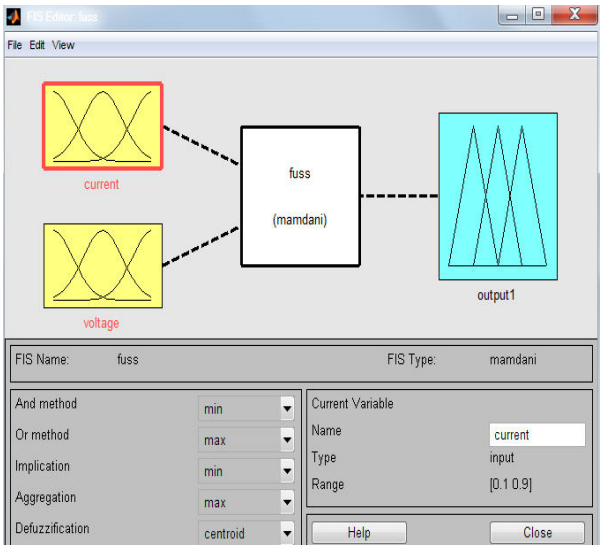


Fig. 9 : Fuzzy rule viewer

The simulation results for MPPT of solar pv system using fuzzy logic controller is shown below

Scheme	Power delivered	Time taken to reach MPPT
Without MPPT	10.05 W	NA
With MPPT using FLC	17.0W	0.02 S

Table 2. Simulation results

VII. CONCLUSIONS

In this paper maximum power point tracking of solar PV is achieved using fuzzy logic controller. The proposed system is explained by using MATLAB simulation model. The control technique used in this paper is more advantages because the tracking of maximum power point is fast in this technique and also sensitive for abrupt changes in solar irradiance. They have the advantage to be robust and relatively simple to design as they do not require the knowledge of the exact model.

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Placement of Multiple Distributed Generators Considering Multi Objective Index Using Linear Programming and Genetic Algorithm

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Abstract - This paper is based on placement of multiple distributed generators (DG) in distribution system. A multi objective index, formulated by combining the appropriately weighed diverse performance indices like voltage profile index, real and reactive power loss index are used to assess the suitable sizes of DG units to be placed. This MOI has been minimized using linear programming and GA optimization tool through Matlab. The simulation study is carried out on a typical 25 bus Indian system and 33 bus system.

Keywords - *Distributed generation, Multi objective index, Voltage stability index.*

I. INTRODUCTION

In the modern world, day by day the load demand increases rapidly due to Industrial and Domestic needs. On the other hand the conventional energy sources are decreasing rapidly. In this case we need an alternative method to meet the load demand, distributed generation is meant for that. It has huge potential benefits about which this paper is concerned.

The distributed generation has been defined by many researchers [1, 2], but in general a distributed generation is nothing but a small generator which is connected at the consumer terminal. Placement of DG is an important factor because improper location may lead voltage instability and power loss. The Newton Rapson load flow method used in [3]. This method reduces the power loss and the cost factor very effectively, but the conventional method of load flow analysis was not applicable for distribution system because of its high R/X ratio, large value of resistance and reactance of the line and radial structure of the distribution system.

TabuGozal used loss sensitivity factor for determination of the optimal size and location of DG to minimize total power loss [4]. Andrew used Linear Programming Technique for placement of DG with multiple constraints [5]. Mallikarjuna used Simulated Annealing for determining the optimal location and size of DG units in a microgrid, given the network configuration and heat and power requirements at various load points [6]. Krueasuk used PSO to find optimal location and size of DG [7]. Lalitha used fuzzy approach to find optimal DG localisation [8].

Hughifam used multi-objective function to minimize cost of energy losses, Investment cost of DG and Operation and maintenance cost. Ochoa minimized real power loss and simple phase short circuit level. Celli used multi objective approach; based on the non-dominated sorbing Genetic Algorithm has been adopted to solve the optimal placement of different types of generation simultaneously. He saved the energy in the form of green house gas emission reduction. Vinoth Kumar addressed minimising the multi objective index using genetic algorithm for the optimal Placement of DG.

This paper minimizes the multi objective index for optimal size of DG and is organized as follows: Section-I: Discussed the load flow analysis of distribution system by Power flow is a crucial part of power system design procedures, and it is categorized into transmission power flow and distribution power flow. The power flow problem consists of a given transmission network where all lines are represented by a Pi-equivalent circuit and transformers by an ideal voltage transformer in series with an impedance. Generators and loads represent the boundary conditions of the solution. In addition, generator or load real and reactive power involves products of voltage and current. However, distribution networks commonly have some special features such as: insufficient information of loads; being radial with sometimes weakly-meshed topology; or high resistance to reactance r/x ratios.

Those features need to be taken into account while carrying out the load flow analysis.

The conventional load flow methods developed essentially for solving transmission networks may encounter convergence problems when applied to distribution networks, due to their high r/x ratio, which deteriorates the diagonal dominance of the Jacobian matrix in the Newton method. Moreover, the loads in distribution networks are distributed and unknowable, since they are always varying with a series of change of daily condition. Therefore, some new methods for distribution systems should be discovered to help solve those issues. Sweep-based algorithms are based on forward-backward sweep processes using Kirchooff's Laws or making use of the well-known bi-quadratic equation which, for every branch, relates the voltage magnitude at the receiving end to the voltage at the sending end and the branch power flow for solution of ladder networks. Due to its low memory requirements, computational efficiency and robust convergence characteristic, sweep-based methods have gained the most popularity for distribution load flow analysis in recent years. Section-II :Discussed different types of DG models. Section-III : Explained the multi objective index and was minimized by linear programming technique. Section-IV: Concludes the paper.

II. LOAD FLOW ANALYSIS

A. *Forward/Backward Sweep Algorithm:*

Although the forward/backward substitution algorithm can be extended to solve systems with loops and distributed generation buses, a radial network with only one voltage source is used here to depict the principles of the algorithm. Such a system can be modeled as a tree, in which the root is the voltage source and the branches can be a segment of feeder, a transformer, a shunt capacitor, or other components between two buses. With the given voltage magnitude and phase angle at the root and known system load information, the power flow algorithm needs to determine the voltages at all other buses and currents in each branch.

The forward/backward substitution algorithm employs an iterative method to update bus voltages and branch currents [9].

This idea is implemented in the proposed algorithm, which consists of the following procedures:

STEP1: Give the slack bus voltage and angle at the root node and initialize voltage equal to the root for all other buses.

STEP 2: The nodal current injections are calculated for all loads using the known power values, *S*, and the latest values of voltages, *V*, computed or assumed.

$$I_i^{[k]} = \left(\frac{S_i^{sch}}{V_i^{[k-1]}} \right)^* \quad (1)$$

Where, [*k*] and [*k*-1] are the current and past iterations of the bus voltage and injected current, *Ii*, at the *i*th bus. Starting from the last branches in the laterals and feeders and moving backwards through the tree to the root node, the algorithm computes the current flowing in all the branches, using the current injections computed.

STEP 3: Then starting from the root with the known slack bus voltage and moving towards the feeder and lateral ends, the voltage at node j is calculated.

$$V_j^{[k]} = V_i^{[k]} - Z_{ij} I_{ij}^{[k]} \quad (2)$$

Where, *Zij* is the branch impedance between buses *i* and *j*, and *Vi* is the latest voltage

STEP 4: The above procedure is repeated until the convergence is satisfied.

III. TYPES OF DG MODEL[11]:

A. *Type-I DG:*

Distributed generator, that supply real power depending on the availability or demand to the network without consuming any reactive power. Such Type-I DG can be modeled as negative constant real power load in the load flow analysis.

B. *Type-II DG:*

Distributed generators, which supply real power to the network only when adequate reactive power support is provided by the network. Such Type-II DG can be an induction generator based fixed speed WTGS.

C. *Type-III DG:*

Type-II DG that is compensated with sufficient local reactive power support, or power electronically controlled using self-commutated converters. Yet their real power outputs are not constant and depend on the connected node voltage. Such Type-III DG can be modelled similar to Type-II DG with the reactive power component set to zero or at desired value.

IV. PROBLEM FORMULATION

A. *OPTIMAL SITING OF DG:*

A system experiences a state of voltage instability when there is a progressive or uncontrollable drop in voltage magnitude following a disturbance, increase in load demand or change in operating condition. It is usually identified by an index called voltage stability index of all the nodes in radial distribution system [4].

$$VSI(n_2)= |V_1|^4 - 4\,[P_2R_1 + Q_2X_1]\,|V_1|^2 - 4\,[P_2X_1 - Q_2R_1]^2 \quad (3)$$

Nodes with minimum voltage instability, in different laterals of the distributed system are chosen as the candidate location for placement of distributed generators.

B. *OPTIMAL SIZING OF DG:*

A multi objective index [1], formulated by combining the appropriately weighed diverse performance indices, is evaluated using linear programming. The following indices are needed to be accomplished simultaneously to achieve optimal operation of the distribution system with DG units.

1) Voltage Profile Index (VPI):

DG placement in the distribution system results in improved node voltages and is defined by an index called voltage profile index given by[5]

$$VPI=\max\left([V_{NOM} - V_i] / V_{NOM}\right)^2 \quad (4)$$

Where V_{NOM} is the nominal system voltage (=1.00 p.u.) and V_i *is* the voltage at node *i.*

2) Real Power Loss Index (PLI):

The change in voltage profile induced by the change in power flows will effect changes in distribution system power loss. Such power losses are required to be minimized, which are measured using the index namely real power loss index is defined by[1]

$$PLI = \frac{P_L}{P_{L-NODG}} \quad (5)$$

Where, P_L and $P_{L\text{-}NODG}$ – are the total real power losses respectively with and without DG in the distribution system.

3) Reactive Power Loss Index (QLI):

The change in voltage profile induced by the change in power flows will effect changes in distribution system power loss. Such power losses are required to be minimized, which are measured using the index namely reactive power loss index defined by[1]

$$QLI = \frac{Q_L}{Q_{L-NODG}} \quad (6)$$

Where, $Q_L$and $Q_{L\text{-}NODG}$ – are the total reactive power losses respectively with and without DG in the distribution system.

4) Line Loading Index (LLI):

With DG placement in the distribution system, there may be an increase or decrease in the line flows at few existing distribution lines, which is addressed using the index called line loading index defined by

$$LLI = \max\left(\frac{S_j}{S_{j-NODG}}\right) \forall j,\ j \in [1, N_b]$$

5) Short Circuit Index (SCI):

The short circuit index (SCI) is related to the protection and selectivity issues arising from the variation of maximum short circuit current contributions before and after placement of DG in the distribution system.

$$SCI = \max\left(\frac{I_{SC_i}}{I_{SC_{i-NODG}}}\right), i \in [2, N_n]$$

V. MULTIOBJECTIVE INDEX (MOI):

The problem of siting and sizing of DG, which is a multiobjective optimization problem, is represented as a multi objective (MOI) as given below by assigning appropriate weights to various performance indices and using weighted sum method.

Minimize MOI= *f*(VPI, PLI,QLI)

Subjected to SCI <SCI_{max}

LLI <LLI_{max}

$$MOI= \alpha_1 VPI + \alpha_2 PLI + \alpha_3 QLI + \alpha_4 SCI + \alpha_5 LLI \quad (7)$$

This MOI equation can be solved using linear programming through MATLAB. This is subjected to the following constraints and limits.

$$\alpha1+ \alpha2\_+ \alpha3 + \alpha4 + \alpha5 =1$$
$$0 \le \alpha1 \le 1$$
$$0 \le \alpha2 \le 1$$
$$0 \le \alpha3 \le 1 \quad (8)$$
$$0 \le \alpha4 \le 1$$
$$0 \le \alpha5 \le 1$$

This MOI equation is minimized for finding the size of the DG to be placed in the distributed system considering the above constraints and limits.

VI. LINEAR PROGRAMMING

A linear programming problem may be defined as the problem of maximizing or minimizing a linear function subject to linear constraints. The constraints may be equalities or inequalities. These problems can be solved by using an optimization tool available in MATLAB. The function to be maximized or minimized is called the objective function. A vector, $\boldsymbol{x}$ for the standard maximum problem or $\boldsymbol{y}$ for the standard minimum problem, is said to be feasible if it satisfies the corresponding constraints. The set of feasible vectors is called the constraint set. A linear programming problem is said to be feasible if the constraint set is not empty; otherwise it is said to be infeasible. A feasible maximum (resp. minimum) problem is said to be unbounded if the objective function can assume arbitrarily large positive (resp. negative) values at feasible vectors; otherwise, it is said to be bounded. Thus there are three possibilities for a linear programming problem. It may be bounded feasible, it may be unbounded feasible, and it may be infeasible. The value of a bounded feasible maximum (resp. minimum) problem is the maximum (resp. minimum) value of the objective function as the variables range over the constraint set. A feasible vector at which the objective function achieves the value is called optimal.

VII. GENETIC ALGORITHM

Genetic algorithms (GAs) are stochastic global search and optimization methods that mimic the metaphor of natural biological evolution. GAs operate on a population of potential solutions applying the principle of survival of the fittest to produce successively better approximations to a solution. At each generation of a GA, a new set of approximations is created by the process of selecting individuals according to their level of fitness in the problem domain and reproducing them using operators borrowed from natural genetics. This process leads to the evolution of populations of individuals that are better suited to their environment than the individuals from which they were created, just as in natural adaptation. GAs has been shown to be an effective strategy in the off-line design of control systems by a number of practitioners. In general, the basic principles of GAs can be characterized by three facts: A set of solution candidates is maintained, which undergoes a selection process and is manipulated by genetic operators, usually recombination and mutation. The GA has evolved and found applications in almost every area of optimization, especially those areas involving problems where the search space is not very well understood. The increasing popularity enjoyed by GA can be attributed in part to its simplicity, elegance, ease of implementation, and its proven ability to often find good solutions for difficult high-dimensional function optimization or combinatorial problems with continuous or discrete variables

VIII. RESULTS AND DISCUSSION

This proposed method of finding location and size of distributed generator is tested on a typical Indian 25 Bus system. The input data for these systems are given in [2]. The load flow solution is obtained for the system. In addition to that, the voltage stability index for all the buses is obtained. Now the bus having least voltage stability index is taken as the location for placing first DG. Solution for load flow analysis of 25 bus system is given in Table1.

TABLE 1

LOAD FLOW SOLUTION WITHOUT DG

BUS NO	VOLTAGE PROFILE	VSI
1	1	1
2	0.9971	0.9862
3	0.9917	0.9666
4	0.9861	0.9457
5	0.9781	0.9128
6	0.9752	0.902
7	0.9729	0.8949
8	0.9689	0.8813
9	0.9681	0.8776
10	0.9667	0.8721
11	0.9619	0.856
12	0.9612	0.852
13	0.9591	0.8437
14	0.9582	0.8395
15	0.9607	0.8506
16	0.96	0.847
17	0.9598	0.8479
18	0.9624	0.8547
19	0.9596	0.8439
20	0.9592	0.8467
21	0.9577	0.8355
22	0.986	0.9449
23	0.9855	0.9414
24	0.9542	0.8243
25	0.9536	0.8252

Values for different indices and multi objective index for different DG sizes are given in table 2 for 25 bus system and table 3 for 33 bus system.

A. Using linear programming

TABLE 2

DIFFERENT INDICES WITH 1st DG FOR 25 BUS SYSTEM

VPI	PLI	QLI	MOI
0.0145	0.1077	0.0354	3.05E-13
0.0145	0.097	0.0354	2.88E-13
0.0145	0.0864	0.0354	2.69E-13
0.0145	0.0757	0.0354	2.48E-13
0.0145	0.065	0.0354	2.26E-13
0.0145	0.0544	0.0354	2.02E-13
0.0145	0.0437	0.0354	1.83E-13
0.0145	0.033	0.0354	1.58E-13
0.0145	0.0224	0.0354	2.41E-13
0.0145	0.0117	0.0354	3.50E-13

TABLE 3

DIFFERENT INDICES WITH 1st DG FOR 33 BUS SYSTEM

VPI	PLI	QLI	MOI
0.0616	0.0018	6.84E-04	7.62E-14
0.0614	0.0016	6.84E-04	7.59E-14
0.0612	0.0014	6.84E-04	7.57E-14
0.061	0.0011	6.84E-04	7.56E-14
0.0609	9.04E-04	6.84E-04	7.55E-14
0.0607	6.78E-04	6.84E-04	7.51E-14
0.0605	4.52E-04	6.84E-04	7.88E-14
0.0603	4.52E-04	6.84E-04	7.84E-14
0.0602	2.26E-04	6.84E-04	7.84E-14
0.06	2.26E-04	6.84E-04	7.80E-14

The size of DG to be placed in that weak bus is selected in such a way that the MOI value is least value.

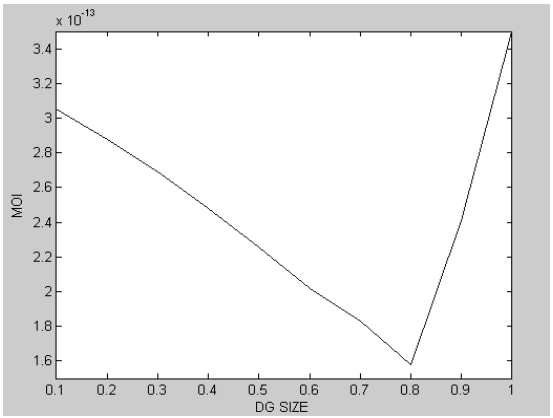

Fig. 1 : Output of linear program (minimized MOI) for 25 bus system

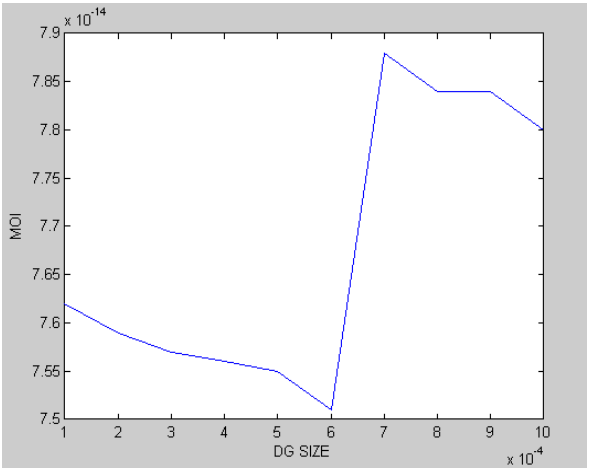

Fig . 2 : Output of linear program (minimized MOI) for33 bus system

From fig 1, 25 bus system it is concluded that the size of DG to be placed in 24th bus is 0.8 MW. After placing the DG in 24th bus, another DG is placed in 25th bus. Again different indices are found for different DG size. This is given in table 4

From fig 2, for 33 bus system, it is concluded that the size of DG to be placed in 22nd bus is 60 kW. After placing the DG in 22nd bus, another DG is placed in 20th bus. Again different indices are found for different DG size. This is given in table 5

TABLE 4

DIFFERENT INDICES WITH 2nd DG FOR 25 BUS SYSTEM

VPI	PLI	QLI	MOI
0.0145	0.0145	0.717	6.15E-16
0.0145	2.3206	0.717	6.02E-16
0.0145	2.2443	0.717	5.88E-16
0.0145	2.1679	0.717	5.74E-16
0.0145	2.0916	0.717	5.58E-16
0.0145	2.0153	0.717	5.42E-16
0.0145	1.9398	0.717	5.25E-16
0.0145	1.8626	0.717	4.91E-09
0.0145	1.7826	0.717	4.73E-09
0.0145	1.7863	0.717	4.53E-09

TABLE 5

DIFFERENT INDICES WITH 2nd DG FOR 33 BUS SYSTEM

VPI	PLI	QLI	MOI
0.0603	8.52E-04	4.73E-04	7.81E-14
0.0602	8.52E-04	4.73E-04	7.78E-14
0.06	7.46E-04	4.73E-04	7.79E-14
0.0598	7.46E-04	4.73E-04	7.77E-14
0.0596	6.39E-04	4.73E-04	7.75E-14
0.0594	6.39E-04	4.73E-04	7.73E-14
0.0593	5.33E-04	4.73E-04	7.71E-14
0.0591	5.33E-04	4.73E-04	7.69E-14
0.0589	4.26E-04	4.73E-04	7.67E-14
0.0587	4.26E-04	4.73E-04	7.64E-14

Values for different indices and multi objective index for different DG sizes are given in table 4 for 25 bus system and table 5 for 33 bus system.

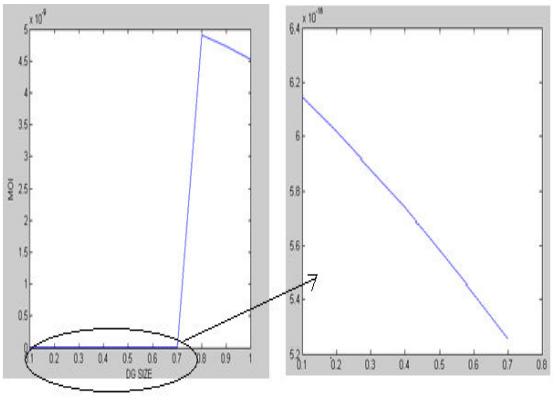

Fig . 3 : Output of linear program (minimized MOI) for 25 bus system

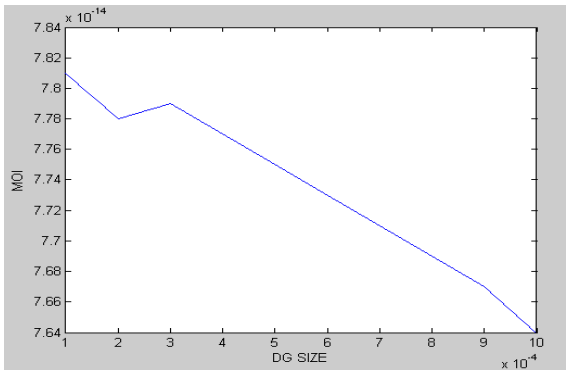

Fig . 4 : Output of linear program (minimized MOI) for 33 bus system

From fig 3, 25 bus system it is concluded that the size of DG to be placed in 25th bus is 0.7 MW. From fig 4, for 33 bus system, it is concluded that the size of DG to be placed in 20th bus is 100 kW.

Table 6 shows the values of weighting factors of different indices obtained using linear programming.

TABLE 6

Weighting factors

INDICES	WEIGHTING FACTOR	WEIGTH
VPI	α1	0.4
PLI	α2	0.2
QLI	α3	0.2
SCI	α4	0.02
LLI	α5	0.18

The voltage profiles of the buses are improved by placing distributed generators in weak buses. First the load flow of the system is done without placing DG. Then after finding the weak bus, first DG is kept that bus. Again another DG is placed in the next weak position. By keeping these DGs in the distributed system, the voltage profile got improved. This is shown in figures 5and 6 for 25 bus system and 33 bus system as follows:

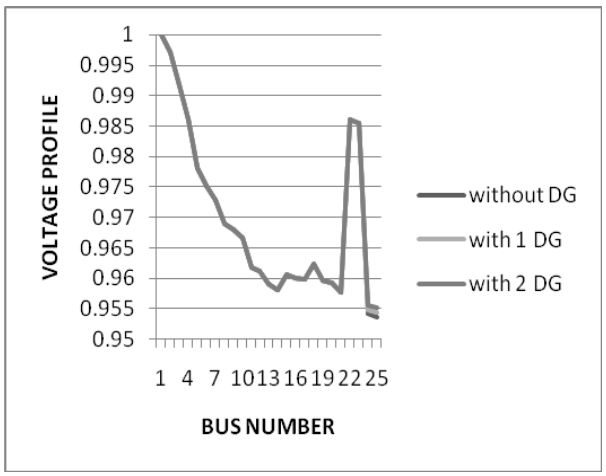

Fig. 5 : Comparison of voltage profile of buses without and with DG for 25 bus system using linear programming

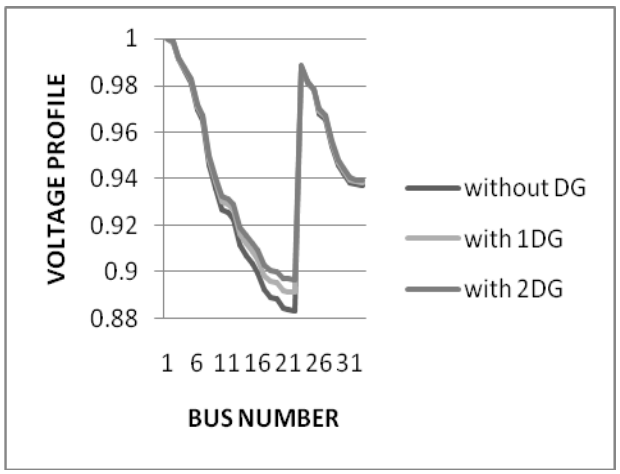

Fig. 6 : Comparison of voltage profile of buses without and with DG for 33 bus system using linear programming

B. Using genetic algorithm

Similarly using genetic algorithm, the location and size of DG can be calculated by minimizing the multi objective index. For 25 bus system, the size of DG to be placed in 5th bus is 1.7 MW and 20th bus is 0.5 MW. For 33 bus system, the size of DG to be placed in 31st bus is 1 MW and 10th bus is 0.1 MW. The improvement in voltage profile after placing DG is shown in fig 7 and 8

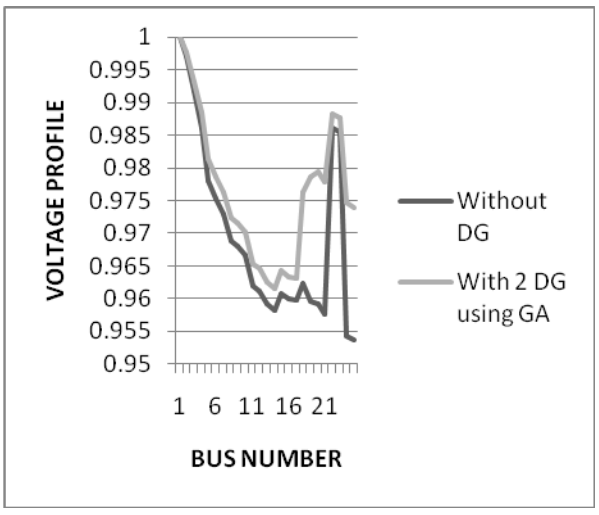

Fig. 7 : Comparison of voltage profile of buses without and with DG for 25 bus system using genetic algorithm

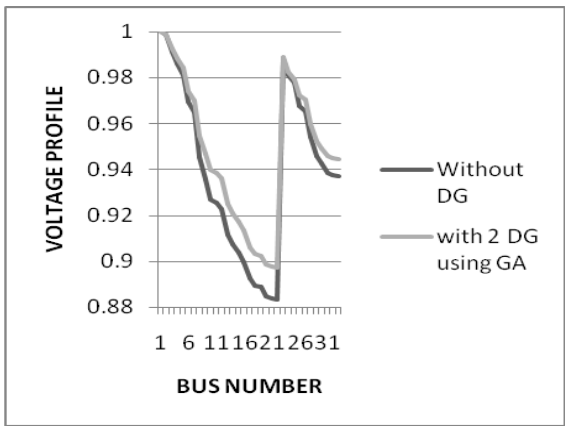

Fig. 8 : Comparison of voltage profile of buses without and with DG for 33 bus system using genetic algorithm

Table 7 shows the values of weighting factors of different indices obtained using genetic algorithm.

TABLE 7 : Weighting factors

INDICES	WEIGHTING FACTOR	WEIGTH
VPI	α1	0.399
PLI	α2	0.199
QLI	α3	0.2
SCI	α4	0.16
LLI	α5	0.041

C. Comparison of LP and GA

The improvement in voltage profile is better if GA is used for finding the location and size of DG. Comparison of the results of genetic algorithm and linear programming is shown in fig 9 and 10.

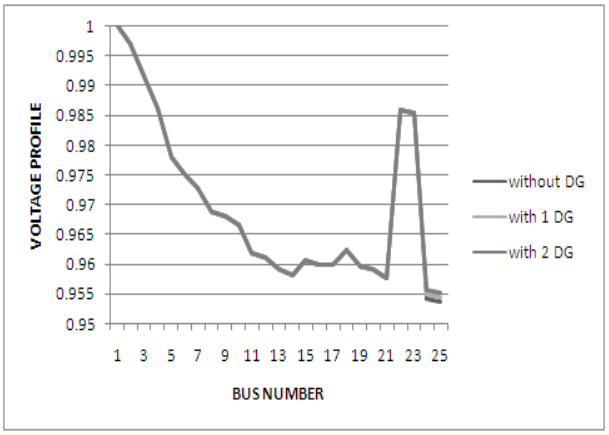

Fig. 9. Comparison of voltage profile of buses without and with DG for 25 bus system using linear programming and genetic algorithm

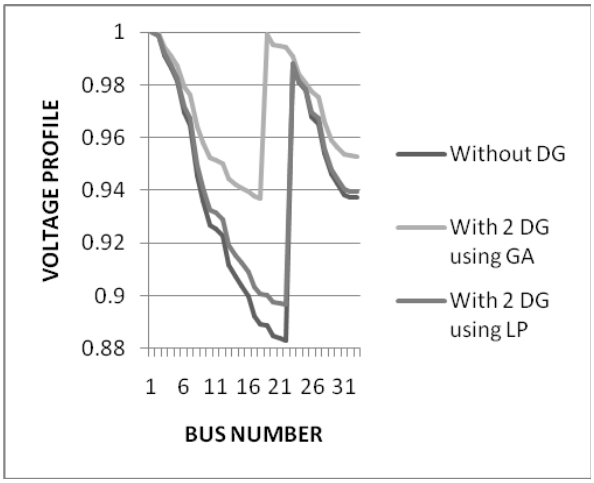

Fig. 10 : Comparison of voltage profile of buses without and with DG for 33 bus system using linear programming and genetic algorithm

IX. CONCLUSION

In this paper, an efficient method is proposed for finding the location and size of Distributed Generator (DG). In this, the location for DG is found using the voltage stability index, through which the voltage profile of the bus system can be improved. The size of DG is found out by minimizing the Multi Objective Index (MOI) using linear programming and genetic algorithm optimization tools in MATLAB. By placing Distributed Generators in distribution system, it is proved that, the voltage profile got improved in the system. The improvement in voltage profile is better if GA is used for finding the location and size of DG.

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A Fractional Delay FIR Filter Based on Lagrange Interpolation of Farrow Structure

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Abstract - An efficient implementation technique for the Lagrange interpolation is derived. This formulation called the Farrow structure leads to a version of Lagrange interpolation that is well suited to time varying FD filtering. Lagrange interpolation is mostly used for fractional delay approximation as it can be used for increasing the sampling rate of signals and systems. Lagrange interpolation is one of the representatives for a class of polynomial interpolation techniques. The computational cost of this structure is reduced as the number of multiplications are minimised in the new structure when compared with the conventional structure.

Keywords - *Farrow structure, Lagrange interpolation, Horner's method, Fractional delay (FD), Finite impulse response (FIR) filter.*

I. INTRODUCTION

A fractional delay filter is a filter of digital type having the main function so as to delay the processed input signal as a fractional of the sampling period time. There are several applications where such fractional signal delay value is required, examples of such systems are: timing adjustment in all-digital receivers (symbol synchronization), conversion between arbitrary sampling frequencies, echo cancellation, speech coding and synthesis, musical instruments modelling etc.

In order to achieve the fractional delay filter function, two main frequency-domain specifications are required by the filter. The filter magnitude frequency response must have an all-pass behaviour in a wide frequency range, as well as it is necessary to have a phase frequency response that must be linear with a fixed fractional slope through the bandwidth.

There are two main design approaches: time-domain and frequency-domain design methods. In first one, the fractional delay filter coefficients are easily obtained through classical mathematical interpolation formulas, but there is a small flexibility to meet frequency-domain specifications. On the other hand, the frequency-domain methods are based on frequency optimization process, and a more frequency specification control is available. One important result of frequency-domain design methods is a highly efficient implementation structure called Farrow structure which allows online fractional value update.

Farrow structure and the modified Farrow structure are two very efficient approaches for adjustable fractional delay filtering, which allows online fractional delay value update with a fixed set of parallel FIR branch filters and only one control parameter. Both structures are composed of L+1 branch FIR filters $C_l(z)$, each one with length N.[3]

II. IDEAL FRACTIONAL DELAY

The continuous-time output signal $y(t)$ of ageneral signal delay system is defined by:

$$y(t) = x(t-t_l) \quad (1)$$

Where x(t) is the continuous-time input signal and $t_l$the obtained time delay value.

In a discrete-time system, the input-output relationship of a signal delay system is expressed as:

$$y(lT) = x(nT-DT) \quad (2)$$

Where the delay value is given by DT, $y(lT)$ and $x(nT)$ are the discrete-time versions of output and input signals, respectively, and T is the sampling period time.

A signal delay value equal to a multiple of the sampling period, D as an integer N, can be easily implemented in a discrete-time system using the signal value for a time of NT:

$$Y(lT) = x(nT-NT) \quad (3)$$

Here the signal delay value is limited to be only N time the sampling period.

The simplified block diagram for a fractional delay filter is shown in fig.1, which output for a non causal FD FIR filter is given by the discrete-time convolution:

$$y(lT) = \sum_{k=N/2}^{\frac{N}{2}-1} x(n-k)h(k,\mu) \qquad (4)$$

Where N is the length of the FD filter. The system function H(z) of the FD filter can be expressed as:

$$H(z) = z^{-D} \qquad (5)$$

Where the delay value is given as: $D = D_{fix} + \mu_l$, $D_{fix}$is a fixed delay value andμ_l is the desired fractional delay value.

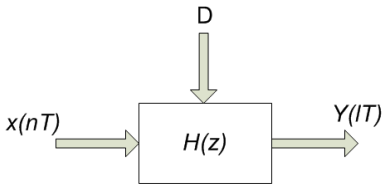

Fig.1 : Simplified block diagram for a FD filter

III. LAGRANGE INTERPOLATION

The Lagrange interpolation method is based on the well-known result in polynomial algebra that using an *N*th-order polynomial it is possible to match N+1 given arbitrary points.

Lagrange interpolation has two favourable features:

1. it is accurate at low frequencies and
2. it never overestimates the amplitude of the signal when the delay has been chosen so that $(N-1)/2 \leq D \leq (N+1)/2$.

The first advantage is justified by the fact that most of the signals are lowpass signals and thus it is advisable to use an approximation technique that has the smallest error at low frequencies.

The second property is called passivity and it implies that the magnitude response of the Lagrange interpolator is less than or equal to one for the mentioned values of D. Always the magnitude response of the Lagrange interpolator exceeds unity when the delay parameter is out of the optimal range.

The use of the Lagrange interpolation method has three main advantages:

1) The easeto compute the FDF coefficients from one closed form equation,
2) The FDF magnitudefrequency response at low frequencies is completely flat,
3) A FDF with polynomial-definedcoefficients allows the use of an efficient implementation structure called Farrow structure.

The magnitude and phase responses of the third-order Lagrange interpolators are shown in fig. 2(a), 2(b).

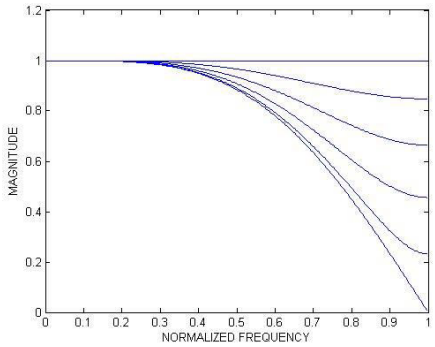

Fig. 2(a) : Magnitude response of Lagrange interpolation

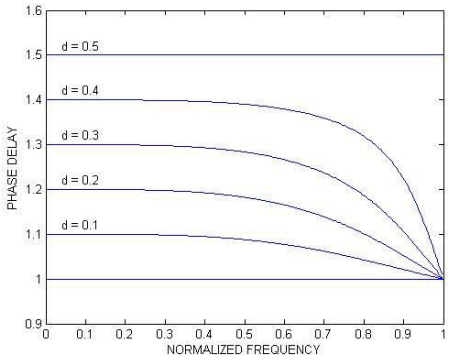

Fig. 2(b) : Phase response of Lagrange interpolation

IV. FARROW STRUCTURE OF LAGRANGE INTERPOLATION

Lagrange interpolation is usually implemented using a direct-form FIR filter structure. An alternative structure is obtained approximating the continuos-time function $x_c(t)$ by a polynomial in D, which is the interpolation interval or fractional delay. The interpolants, i.e., the new samples, are now represented by

$$y(n) = x(n-D) = \sum_{k=0}^{N} c(k)D^k \qquad (6)$$

That takes on the value $x(n)$ when $D = n$. The coefficients $c(k)$ are solved from a set of N+1 linear equations. Farrow has suggested that every filter

coefficient of an FIRinterpolating filter could be expressed as an *N*th-order polynomial in the delay parameter*D*. Hence this result in *N*+1 FIR filters with constant coefficients.

The alternative implementation for Lagrange interpolation is obtained formulatingthe polynomial interpolation problem in the z-domain as

$$Y(z) = H(z)X(z) \quad (7)$$

Where X(z) and Y(z) are the z-transforms of the input and output signal, x(n) and y(n),respectively, and the transfer function H(z) is now expressed as a polynomial in D.

$$H(z) = \sum_{k=0}^{N} C_k(z)\, D^k \quad (8)$$

The familiar requirement that the output sample should be one of the input samples forinteger D may be written in the z-domain as

$$Y(z) = z^{-D}X(z) \text{ for } D = 0,1,2,K,N \quad (9)$$

Together with Eqs. (8) and (9) this leads to the following N + 1 conditions

$$\sum_{k=0}^{N} C_k(z)\, D^k = z^{-D} \; for\; D = 0,1,2 \ldots N \quad (10)$$

This may be expressed in matrix form as

$$Uc = z \quad (11)$$

Where the L×L matrix U is given by

$$U = \begin{bmatrix} 0^0 0^1 & 0^2 & \cdots & 0^N \\ 1^0 1^1 & 1^2 & \cdots & 1^N \\ 2^0 2^1 & 2^2 & & 2^N \\ \vdots & & \ddots & \vdots \\ N^0 N^1 & N^2 & \cdots & N^N \end{bmatrix} = \begin{bmatrix} 10 & 0 & & 0 \\ 11 & 1 & \cdots & 1 \\ 12 & 4 & & 2^N \\ \vdots & & \ddots & \vdots \\ 1\,N & N^2 & \cdots & N^N \end{bmatrix} \quad (12)$$

vector c is

$$c = [C_0(z) C_1(z) C_2(z) \;\ldots\; C_N(z)]^T \quad (13)$$

and the delay vector

$$z = [1 \;\; z^{-1} z^{-2} \;\ldots\; z^{-N}]^T \quad (14)$$

The matrix **U** has the Vandermonde structure and thus it has an inverse matrix $\mathbf{U}^{-1}$.

The solution of Eq. can thus be written as

$$c = U^{-1}z \quad (15)$$

The inverse matrix $\mathbf{U}^{-1}$, that we shall denote by **Q**, may be solved using Cramer's rule.

The rows of the inverse Vandermonde matrix **Q** contain the filter coefficients used inthe new structure, and thus it is convenient to write

$$Q = [q_0 q_1 q_2 \;\ldots\; q_N]^T \quad (16)$$

The transfer functions *Cn*(*z*) are thus obtained by inner product as

$$C_n(z) = q_n z = \sum_{k=0}^{N} q_n(k)\, z^{-k} \; for\; n = 1,2, \ldots N \quad (17)$$

The coefficients *qn*(*k*) for the FIR filters *Cn*(*z*) are computed inverting the Vandermondematrix **U**.

By setting *D* = 0 in Eq. (10), it is seen that

$$\sum_{k=0}^{N} C_k(z)\, 0^k = 1 \;\Rightarrow C_0 \equiv 1 \quad (18)$$

This implies that the transfer function $C_0(z) = 1$ regardless of the order of the interpolator.

The other transfer functions *Cn*(*z*) given by Eq. (17) are *N*th-order polynomials in*z*-1 , that is, they are *N*th-order FIR filters. The interpolator is directly controlled by the fractional delay D, i.e., no computationally intensive coefficient update is needed when D is changed.

Farrow structure is most efficiently implemented using Horner's method that is

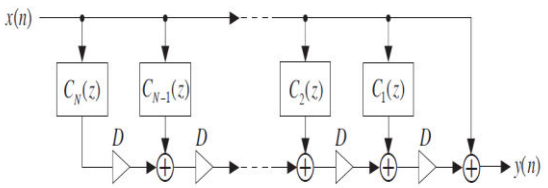

Fig. 3 : Farrow structure of Lagrange interpolation implemented using Horner's method.

$$\sum_{k=0}^{N} C_k(z)\, D^k = C_0(z) + [C_1(z) + [C_2(z) + \cdots + [C_{N-1}(z) + C_N(z)D]D \ldots]D \quad (19)$$

In this method *N* multiplications by *D* are needed. A general *N*th-order Lagrangeinterpolator that employs the suggested approach is shown in Fig. 3. Since there isno need for the updating of coefficients, this structure is particularly well suited toapplications where the fractional delay *D* is changed often, even after every sampleinterval.

If the delay is constant or updated very seldom, it is recommended to implementLagrange interpolation using the standard FIR filter structure because it is computationallyless expensive. Namely, with the FIR filter structure $N + 1$ multiplications and$N$ additions are needed. In Farrow's structure, there are N pieces of Nth-order FIR filterswhich results in $N(N+1)$ multiplications and N^2 additions. There are also N multiplicationsby D and N additions. Altogether this means $N^2+ 2N$ multiplications and$N^2+ N$ additions per output sample.

As examples, let us solve for the transfer functions $C_n(z)$ for linear interpolation andsecond-order Lagrange interpolation. For $N = 1$, Eq. (11) yields

$$\begin{bmatrix}0 & 1\\ 1 & 1\end{bmatrix}\begin{bmatrix}C_0(z)\\ C_1(z)\end{bmatrix} = \begin{bmatrix}1\\ z^{-1}\end{bmatrix} \tag{20}$$

The solution is given by

$$\begin{bmatrix}C_0(z)\\ C_1(z)\end{bmatrix} = \begin{bmatrix}1 & 0\\ 1 & 1\end{bmatrix}^{-1}\begin{bmatrix}1\\ z^{-1}\end{bmatrix} = \begin{bmatrix}1 & 0\\ -1 & 1\end{bmatrix}\begin{bmatrix}1\\ z^{-1}\end{bmatrix} = \begin{bmatrix}1\\ -1+z^{-1}\end{bmatrix} \tag{21}$$

It is seen that $C_1(z) = z^{-1}$-1 when $N = 1$. The overall transfer function $H(z)$ of theFarrow structure of linear interpolation is written as

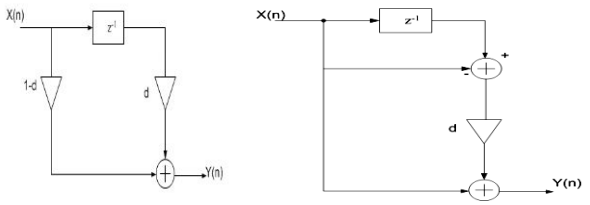

Fig. 4(a) : The direct-form FIR filer structure for linear interpolation and Fig. 4(b) the equivalent Farrow structure

$$H(z) = 1 + (z^{-1} - 1)D \tag{22}$$

Note that in this case $D = d$. The linear interpolator may thus be implemented by the structure illustrated in Fig. 4b. It is seen that the Farrow structure is as efficient as the direct-form non-recursive structure (Fig. 4a) when $N = 1$, since the number of operations is the same in both. If multiplication is more expensive than addition, like it is in VLSI implementations, then the Farrow structure (Fig. 4b) is preferable.

For N = 2 eq. is written as

$$\begin{bmatrix}1 & 0 & 0\\ 1 & 1 & 1\\ 1 & 2 & 4\end{bmatrix}\begin{bmatrix}C_0(z)\\ C_1(z)\\ C_2(z)\end{bmatrix} = \begin{bmatrix}1\\ z^{-1}\\ z^{-2}\end{bmatrix} \tag{23}$$

Now the inverse vandermonde matrix Q is given by

$$Q = U^{-1} = \begin{bmatrix}1 & 0 & 0\\ -3/2 & 2 & -1/2\\ 1/2 & -1 & 1/2\end{bmatrix} \tag{24}$$

The transfer functions thus obtained are

$$C_0(z) = 1, C_1(z) = -\frac{3}{2} + 2z^{-1} - \frac{1}{2}z^{-2},\ C_2(z) = \frac{1}{2} - z^{-1} + \frac{1}{2}z^{-2} \tag{25}$$

And the overall transfer function H(z) can be written as

$$H(z) = C_0(z) + C_1(z)D + C_2(z)D^2 \tag{26}$$

Farrow form of parabolic or second-order Lagrange interpolation is illustrated in Fig. 5. In this example it is seen that the transfer functions $C_n(z)$ can share unit delays, because they all use the same delayed signal values $x(n - k)$ with $k = 0, 1, 2, ...,N$. Furthermore, the number of multiplications can be reduced in a practical implementation.It may be taken into account that some of the coefficients have the value 1 or -1thus eliminating the need for a multiplication and that the corresponding coefficients of two transfer functions can be equal.

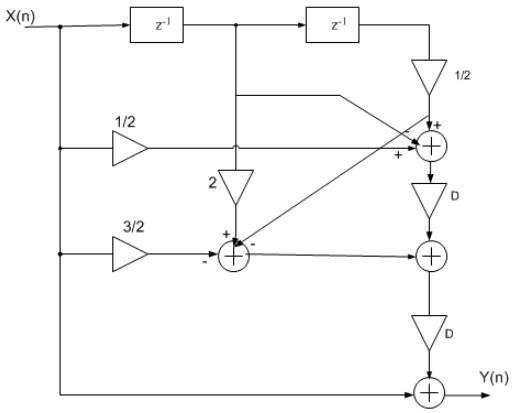

Fig. 5 : Farrow structure for a second order Lagrange interpolator

Modified Farrow structure

Farrow structure can be made more efficient changing the range of the parameter Dso that the integer part is removed. The new parameter range is $0 \le d \le 1$ (for odd N) or$-0.5 \le d \le 0.5$ (for even N). This change can

be obtained introducing a transformationmatrix **T** defined by

$$T_{n,m} = \begin{cases} round\left(\frac{N}{2}\right)^{n-m}\left(\frac{n}{m}\right) \; for\; n \geq m \\ 0 \; for\; n < m \end{cases} \quad (27)$$

Where $n, m = 0, 1, 2, ..., N$

For $N = 2$ this matrix is expressed as

$$T = \begin{bmatrix} 1 & 1 & 1 \\ 0 & 1 & 2 \\ 0 & 0 & 1 \end{bmatrix} \quad (28)$$

Multiplying the coefficient matrix **Q** by matrix (3.110) a modified coefficient matrix is obtained as

$$\boldsymbol{Q} = \boldsymbol{TQ} = \begin{bmatrix} 1 & 1 & 1 \\ 0 & 1 & 2 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} 1 & 0 & 0 \\ -3/2 & 2 & -1/2 \\ 1/2 & -1 & 1/2 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -1/2 & 0 & 1/2 \\ 1/2 & -1 & 1/2 \end{bmatrix} \quad (29)$$

This transformation is equivalent to substituting $D' = D + 1$. The FIR filters of themodified structure are written as

$$\mathfrak{C}_0(z) = z^{-1}, \mathfrak{C}_1(z) = -\frac{1}{2} + \frac{1}{2}z^{-2}, \mathfrak{C}_2(z) = \frac{1}{2} - z^{-1} + \frac{1}{2}z^{-2} \quad (30)$$

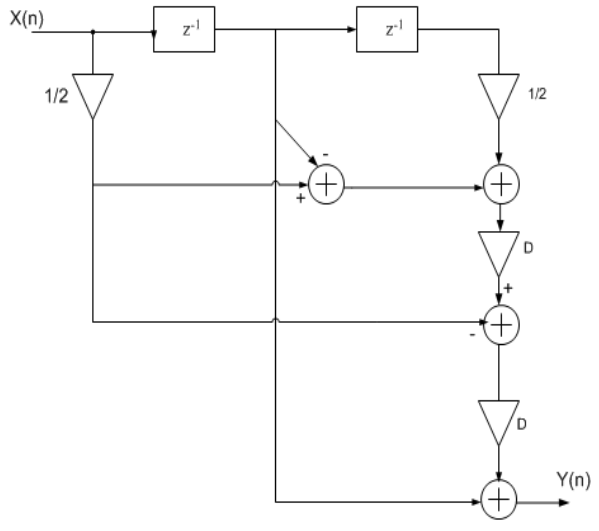

Fig. 6 : Modified Farrow structure for a second order Lagrange interpolator.

V. RESULTS

Table 1 represents the arithmetic complexity for the various orders of the Farrow structure of Lagrange interpolation. The usage of multipliers and adders are tabulated below as follows:

TABLE I

Order of the Farrow structure	Adders	Multipliers
Second order	6	6
Modified second order	4	4

Table II and III represents the optimization results for various FD FIR filters.

TABLE II

Order of the Farrow structure	Area (μm^2)	Cell count	Power (µw)	Delay (ns)
First order	4264	358	1.63	2.47
Second order	10100	931	3.55	3.32
Modified second order	9999	900	3.03	3.24

TABLE III

FD FIR filter	Area (μm^2)	Power (µw)	Delay (ns)
Horner's method	3568	1.13	5.367
Modified Second order Farrow	4832	0.78	0.323

VI. CONCLUSIONS

In this paper an efficient technique for the FD FIR filter has been proposed using the Lagrange interpolation of the Farrow structure. Lagrange interpolation is preferable for the applications where a low order FD filter is needed. A new implementation structure of the Farrow structure based Lagrange interpolation is derived. Farrow structure of Lagrange interpolation is being compared with the modified Farrow structure of Lagrange interpolation and it is noticed that the complexity, power and delay is optimized.

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Fetal Phonocardiogram Signal Acquisition & Analysis

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Abstract - Fetal Phonocardiography is a simple and non-invasive diagnostic technique for surveillance of fetal well-being. The fetal phonocardiographic (fPCG) signals carry valuable information about the anatomical and physiological state of the fetal heart [5]. In this technique the vibro acoustic signals of diagnostic importance can be conveniently captured from the surface of mother's abdomen by placing a small and inexpensive acoustic sensor. Then phonocardiographic signal fed to computer with the help of 8051 microcontroller (AT89C51) via RS232.

Keywords - *Electronic fetal monitor, Hearts sound, phonocardiography, DAQ, signal processing.*

I. INTRODUCTION

Earlier fetal monitoring was used for complicated and 'high-risk' pregnancies only. However due to advancements in technology and ease of operation the same is gradually used in the 'low-risk' pregnancies also. The most common method for fetal monitoring is recording and monitoring of fetal heart rate (FHR) and analysis of fetal heart rate variability (fHRV). FHR trace is a time versus heart rate in beats per minute (bpm) waveform derived from the fPCG signal, and provides a picture of overall heart activity for a considerably longer span of time. FHRV analysis has a physiological significance because changes in FHR are coupled to fetal well-being.

II. ELECTRONIC FETAL MONITORING

Electronic fetal monitoring (EFM) is a method for examining the condition of an unborn in the uterus by noting any unusual changes in its heart rate. 'Fetal monitoring' in a wide sense means fetal surveillance but, practically, it is an indirect way to measure fetal well-being or the adequacy of fetal oxygenation and, as such, it is an integral part of the concept of 'the fetus as a patient'. The primary goal of fetal monitoring is a healthy newborn with a healthy mother.

A variety of non-invasive techniques are used for the purpose of fetal monitoring. The fetus is mechanically shielded from outside world so that it can be safely developed in uterus. Thus, only the limited amount of information can be directly obtained about the fetal condition. This information is in the form of various signals picked up from maternal abdominal wall, and they are:

- Electrical potential caused by the bioelectric activity of fetal heart.
- Magnetic field caused by the bioelectric activity of fetal heart.
- Acoustic Vibrations caused by the mechanical activity of fetal heart.

Based on the detection of these signals, the methods that are commonly employed in EFM are fetal electrocardiography (fECG), continuous wave ultrasound Doppler-shift based fetal cardiotocography (fCTG) and fetal magnetocardiography (fMCG).

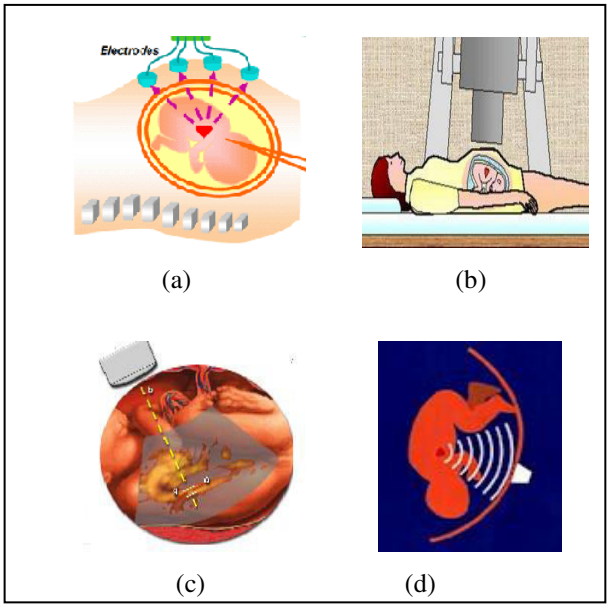

Fig. 1: (a)fECG, (b)fMCG, (c)fCTG, (d)fPCG

These techniques provide good results but require expensive equipment, specialized technicians to operate, experts to interpret the results, high maintenance cost, permanent placement, and generally demand more resources to function properly. These requirements can only be met in the advanced hospitals and are way beyond the reach of rural healthcare centers as well as for urban clinics.7 On the other hand, fetal phonocardiography (fPCG) is a low-cost, non-invasive (passive), and simple technique in comparison to the widely accepted Doppler ultrasound examination. It is a suitable tool for long-term surveillance of the fetus [**2**].

III. FETAL PHONOCARDIOGRAPHY

Fetal Phonocardiogram is a time versus amplitude plot of fetal heart sound and is considered as the primary time domain characteristic of the fetal heart sound signal. It is a graphical representation of vibration or sound signal detected from the maternal abdominal wall, caused by the contractile activity of the fetal heart.

Heart sound analysis provides important information related to heart condition, which plays an important role in the diagnosis of cardiovascular disorders [1]. Heart sounds, or heartbeats, are the noises generated by the beating heart and the resultant flow of blood through it. These are the first heart sound (S_1) and second heart sound (S_2), produced by the closing of the AV valves and semi lunar valves respectively.

In addition to these normal sounds, a variety of other sounds may be present including heart murmurs, S_3 and S_4.

A third low frequency sound (S3) may be heard at the beginning of the diastole, during the rapid filling of the ventricles. A fourth heart sound (S4) may be heard in the late diastole during atrial contraction, which are generally inaudible.

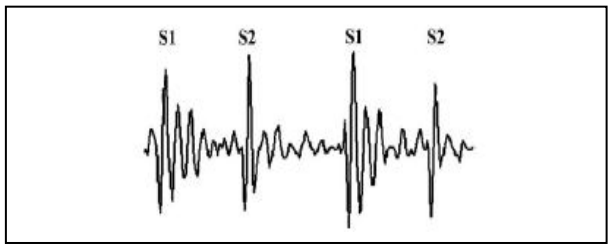

Fig. 2 : Heart Sounds

IV. SYSTEM DESCRIPTION

DATA ACQUISITION

The fetal heart sound is in the form of mechanical vibrations passing through tissue structures. These vibrations are relatively weak because of the physical distance and small size of the fetal heart valve. In order to sense this weak heart sound from the maternal abdomen, the transducer should be highly sensitive, accurate, and properly placed. For this purpose, a phonocardiography-based data acquisition system is specially developed. The block diagram of the data acquisition system is shown in Fig.

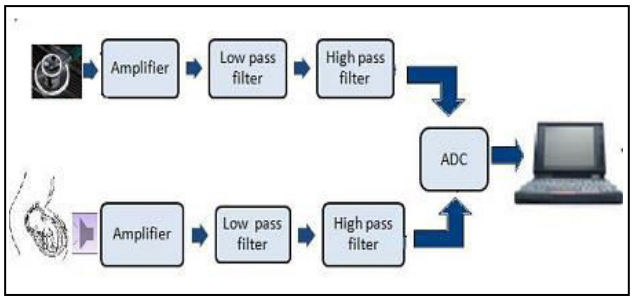

Fig. 3 : Data acquisition system

Fetal phonocardiography requires the conversion of mechanical vibration on subject's abdomen to electrical signal by microphone. Fetus heart sound is extremely weak hence it cannot be sensed properly by putting a sensor immediately on the subject's abdomen. To overcome this problem a particular acoustic cone is developed which is a direct extension of the chest piece of standard stethoscope. The air enclosed in the cone acts as a transmission media between the membrane and electro-mechanical transducer device. [1] Here, we capture maternal signal only through this acquisition system and we generate simulated signal for fetal.

SIGNAL CONDITIONING

The output of the sensor is fed to signal conditioning circuit. Instrumentation Amplifier is used here for this particular purpose, which raises the signal from the transducer level to the line level [1].

It is essential to keep ambient noise as low as possible; this is carried out by 4^{th} low pass filter with cut-off frequency of 200 Hz. This value of cut off frequency is selected, because most of the fetus heart sound spectrum lies below this frequency limit. Active filter is implemented using an easily available operational amplifier IC TL082 along with suitable resistor capacitor net-work.

For DC Drift removal 4^{th} order High pass Filter with 10 Hz cut off frequency is used. To remove line frequency noise of 50Hz Notch filter is used. For the Analog Signal Filtering TL082 is used, because of its Low power consumption and High Input Impedance Characteristics.

SOFTWARE AND HARDWARE INTERFACING

The goal of Digital Signal Processing is usually to measure, filter and/or compress continuous real-world

analog signals. The first step is usually to convert the signal from an analog to a digital form, by sampling and then digitizing it using an analog-to-digital converter (ADC), which turns the analog signal into a stream of numbers.

Fig. 4 : Signal interfacing with PC

We describe the interfacing of 8051 microcontroller (AT89C51) with a computer via serial port, RS232.

RESULTS

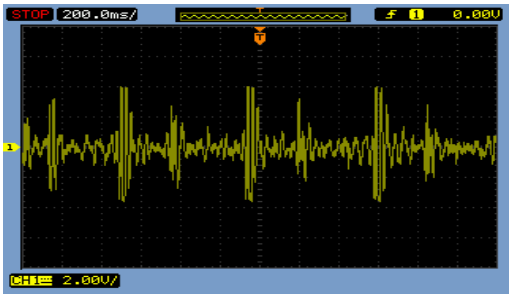

Fig. 5 : First & second heart sound

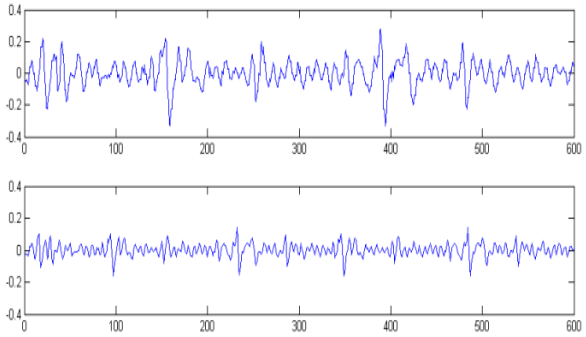

Fig. 6 : Maternal and simulated fetal first & second heart sounds

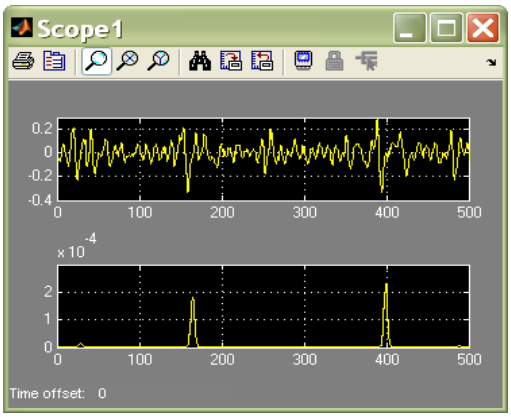

Fig. 7 : Envelope detection of maternal signal

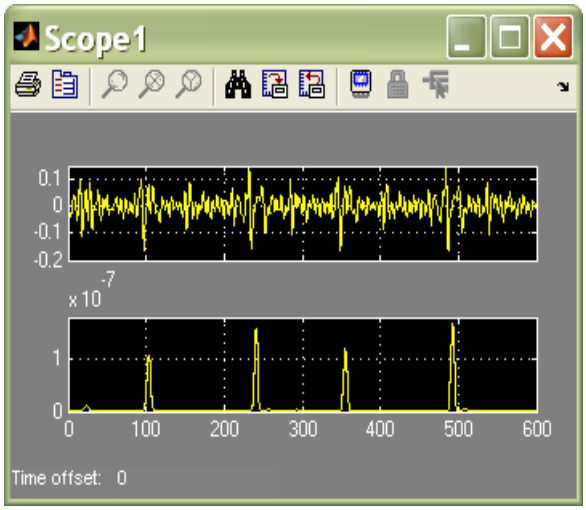

Fig. 8 : Envelope detection of fetal signal

Figure 5 is the final phonocardiographic signal, which the instrument provides. Figure 6 shows maternal signal and simulated fetal signal. Figure 7 & 8 is signal envelope provided by the complex process of envelope generation of maternal and fetal signal respectively.. This envelope is then passed through an amplitude thresholding process that in turn converts amplitude burst of the envelope signal into discrete pulses. Then the final processed signal used for the FHR calculation.

V. CONCLUSION:

Fetal Phonocardiography is a simple and non-invasive diagnostic technique for surveillance of fetal well-being. Here we generally acquire maternal phonocardiogram signal through this system and generate simulated signal for fetal. After that we used matlab simulik to generate simulink model for envelope of both the signal. Then we calculate the heart rate of both signals. From experiment we know that maternal heart rate is around 70-80 bpm while normal fetal heart rate is in the range of 120-160 bpm.

VI. ACKNOLEDGEMENT

I would like to express my sincere thanks to Prof. J.B.Vyas, Head of Biomedical Engineering Department, and Govt. Engg. College, Gandhinagar for this guidance, encouragement and support during my work. Despite his busy schedule, he is always available to give me advice, support and guidance during the entire period. I would like to express my sincere thanks to all my friends and all faculty members of Biomedical Department for their help and suggestions during my work.

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Economic Load Dispatch with Pollution Problems Using Particle Swarm Optimization

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Abstract - This paper presents a particle swarm optimization (PSO) method for solving the Economic load dispatch with pollution problems (ELDPP) of thermal units while satisfying the constraints such as generator capacity limits, power balance and line flow limits. The objective is to minimize the total fuel cost of generation and environmental pollution caused by fossil based thermal generating units and also maintain an acceptable system performance in terms of limits on generator real power outputs, transmission losses. The proposed approach has been evaluated on an IEEE 30-bus test system with six generators. The results obtained with the proposed approach are compared with results of genetic algorithm and other technique.

Keywords - *Economic Load Dispatch, Pollution Control, NOx emission, Particle Swarm Optimization.*

I. INTRODUCTION

This paper work deals with the economic problem namely the economic thermal power dispatch with emission dispatch due to toxic gases. In seeking the solution for the economic dispatch problem with pollution problems (ELDPP) the main aim is to operate a power system in such a way to supply all the loads at the minimum cost. The solution technique which is applied to the ELDPP is particle swarm optimization (PSO) method. In electric power system operation, the objective is to achieve the most economical generation policy that could supply the local demands without violating constraints. Thermal stations, during power production, burn fossil fuels that generate toxic gases in their effluent and these become a source of pollution for the environment. The ELDPP calculation optimizes the static operating condition of a power generation-transmission system with security of quality of service.

The ELDPP has been usually considered as the minimization of an objective function representing the generation cost and/or the transmission loss. The constraints involved are the physical laws governing the power generation-transmission systems and the operating limitations of the equipment.

One of the most recent metaheuristic algorithms, the Particle Swarm Optimization (PSO), is a population based stochastic optimization technology [9, 10] by Eberhart and Kennedy in 1995, inspired by social behaviour of bird flocking and fish schooling. It is used for optimization of continuous non linear functions [11, 12]. PSO is applied to different areas of power systems to minimize real power system losses [13]. The proposed approach has been examined and tested on the standard IEEE 30-bus test system with different objectives that reflect fuel cost minimization, voltage profile improvement, and voltage stability enhancement.

The PSO is a swarm intelligence algorithm, inspired by the social dynamics and emergent behaviour that arises in socially organized colonies. The PSO algorithm exploits a population of individuals to probe promising regions of search space. In this context, the population is called swarm, and the individuals are called particles or agents. Each particle moves with an adaptable velocity within the regions of search space and retains a memory of the best position it ever encountered. The rest position ever attained by each particle of the swarm is communicated to all other particles [22]. The concept of PSO originated as a simulation of a simplified social system. This method is based on researches about swarms such as fish schooling and a flock of birds. According to the research results for a flock of birds, birds find food by flocking (not by each individual).

According to the observation of behaviour of people during a decision process, people utilize two important kinds of information. The first one is their own experience; that is, they have tried the choices and know which state has been better so far, and they know how good it was. The second one is other people‟s experiences; that is, they have knowledge of how the

other individuals (agents) around them have performed. They know which choices of their neighbours have been found as more positive and also the positiveness of the pattern. Each agent decides the decision using individual experiences and other people‟s experiences [23].

In recent years, environmental constraint started to be considered as part of electric system planning. That is, minimization of pollution emission (NOx, SOx, CO2, etc.) in case of thermal generation power plants. However, it became necessary for power utilities to count this. Constraint as one of the main objectives, which should be solved together with the cost problem. Thus, we are faced with a multi-objective problem.

Spens and Lee [24] solved the economic load dispatch under environmental restrictions in a multi-hour time horizon minimizing fuel consumption cost for SO2 and NOx using an emission ton limit for the first one and an emission rate for the second one.Fan and Zhang [25] solved a cost minimization problem proposing a solution via quadratic programming, where environmental restrictions are modelled with linear inequalities.

In a previous paper [26], the authors proposed the use of a genetic algorithm with real coding on the ELDPP problem using as objective function the minimization of the fuel cost and NOx emission control. More than 6 small-sized test cases were used to demonstrate the performance of the proposed algorithm. Consistently acceptable results were observed In a recent paper [27], the authors presented the application of the Particle Swarm Optimization (PSO) method to the Optimal Power Flow problem for a large scale power system. The objective function considers at the same time the cost of the power generation, the transmission loss and the voltage deviation. Numerical results for IEEE 30-bus test systems show that a PSO technique can generate an efficiently high quality solution and with more stable convergence characteristics than genetic algorithms (GA).

II. PROBLEM FORMULATION

The optimization of cost of generation has been formulated based on economic dispatch with emission and line flow constraints. For a given power system network, the optimization cost of generation is given by the following equation.

a. Economic Objective Function : The most commonly used objective „Economic Load Dispatch with pollution‟ problem formulation is the minimization of the total operating cost of the fuel consumed for producing electric power within a schedule time interval.

$$F = \sum_{i=1}^{N_g}(a_i + b_i P_{g_i} + c_i P_{g_i}^2) \quad (1)$$

where

F-is fuel cost of i^{th} generator in $/hr.

Pg_i-is the generator power output of i^{th} generator in MW.

i- represents the corresponding generator (1,2,.....n)

N_g- represents number of generators.

a_i,b_i,c_i- are the fuel cost coefficients.

The equation (1) is subjected to the following constraints:

i. The inequality constraints on real power generation Pg_i of each generation i.

$$P_{g_i}^{min} \leq P_{g_i} \leq P_{g_i}^{max} \quad (2)$$

Where $P_{g_i}^{min}$ and $P_{g_i}^{max}$ are respectively minimum and maximum values of real power generation i.

ii. The cost is optimized with the following power system balance constraints.

$$\sum_{i=1}^{N_g} P_{g_i} = P_D + P_L \quad (3)$$

Where

Pg_i -is the real power generation of i^{th} generator.

P_D - is the load of the system in MW.

P_L - is the transmission loss of the system in MW.

N_g- is the total number of generators.

iii. The total transmission network losses the power system is obtained by

$$P_L = B_{oo} P_{g_i} + \sum_{i=1}^{N_g}\sum_{j=1}^{N_g} P_{g_i} B_{ij} P_{g_j} \quad (4)$$

Where

B_{oo},B_{ij},B_{oi} - are the transmission loss coefficientsm i,j represent the number of lines.

b. Emission objective function: The total emission release can be expressed as –

$$E_i(P_{g_i}) = a_i P_{g_i}^2 + \beta_i P_{g_i} + \gamma_i \quad (5)$$

Where

E_i - Total emission release in kg/hr

P_{gi} - is the generator power output of the it generator in MW

i – represents the corresponding generator (1,2,.....n)

N_g - Total number of generator

$\alpha_i,\beta_i,\gamma_i$ - are NO_x emission coefficients.

To determine the combined effect of cost and emission, the price penalty factor has to be computed. It blends the generation and emission cost into single objective nature. The price penalty factor is computed by interpolating the values of h_i for last two units by satisfying the corresponding load demand and it is given by the relation (considering the power associated with each unit).The resulting array elements are arranged in ascending order , after arranging the maximum power of each unit is added one at a time starting from the smallest price penalty factor unit until the summation equals or exceeds the power demand. The price penalty factor at the unit when added exactly meets or exceeds the demand is represented as h_{i2} and the price penalty factor of the previous unit is represented as h_{i1} in recent analysis of venkatesh et al. have shown that this method of calculation of price penalty factor furnished good result and it is represented by the following equation-

$$Z = h_{i\,1} + \left(\frac{h_{i\,2} - h_{i\,1}}{P_{max\,2} - P_{max\,1}}\right) * (P_D - P_{max\,1}) \quad (6)$$

Where

Z - Price penalty factor in $/Kg.

h_{i1}- Price penalty factor associated with the last unit in $/Kg.

h_{i2} – Price penalty factor with the current unit in $/Kg.

P_{max1} - maximum power associated with the last unit in MW.

P_{max2} - maximum power associated with the current unit in MW.

c. Total objective function : The economic dispatch and emission dispatch are considerably different. The economic dispatch deals with only minimizing the total fuel cost (operating cost) of the system violating the emission constraints. On the other hand emission dispatch deals with only minimizing the total emission of NOx from the system violating the economic constraints. Therefore it is necessary to find out an operating point, that strikes a balance between cost and emission. This is achieved by combined economic and emission dispatch (CEED).The multi-objective combined economic and emission dispatch problem is converted into single optimization problem by introducing price penalty factor$Z$.

Minimize $\varphi = F + Z * E$ (Rs./hr) (7)

III. PARTICLE SWARM OPTIMIZATION

a. Description of Particle Swarm Optimization method

Kennedy and Eberhart developed a PSO algorithm based on the behaviour of individuals (i.e., particles or agents) of a Swarm [11]. Its roots are in zoologist‟s modelling of the movement of individuals (i.e., fish, birds, and insects) within a group. It has been noticed that members of the group seem to share information among them, a fact that leads to increased efficiency of the group. The PSO algorithm searches in parallel using a group of individuals similar to other AI-based heuristic optimization techniques [12]. Each individual corresponds to a candidate solution to the problem. Individuals in a swarm approach to the optimum through its present velocity, previous experience, and the experience of its neighbours. The particle swarm optimization works by adjusting trajectories through manipulation of each coordinate of a particle. Let $i\ x$ and $i\ v$ denote the positions and the corresponding flight speed (velocity) of the particle i in a continuous search space, respectively.

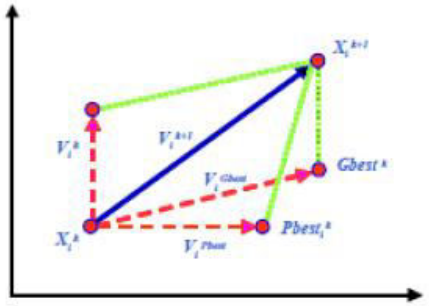

Fig. 2. Concept of modification of a searching point by PSO.

The particles are manipulated according to the following equations.

$$v_i^{(r+1)} = w.v_i^{(t)} + c_1.r_1.\left(x_{gbest}^{(t)} - x_i^{(t)}\right) + c_2 * r_2 * \left(x_{ipbest}^{(t)} - x_i^{(t)}\right) \quad (9)$$

$$x_i^{(t+1)} = x_i^{(t)} + v_i^{(t+1)} \quad (10)$$

Where:

t: pointer of iterations (generations).

w: inertia weight factor.

c1, c2: acceleration constant.

r1, r2: uniform random value in the range (0, 1). (t)

$v_i^{(t)}$: Velocity of particle i at iteration t.

$x_i^{(t)}$: current position of particle at iteration t.

$x_{ipbest}{}^t$: previous best position of particle t at iteration t.

$x_{gbest}{}^t$: best position among all individuals in the population at iteration t.

$v_i^{(t+1)}$): new velocity of particle i.

$x_i^{(t+1)}$: new position of particle i.

b. PSO applied to ELDPP

Our objective is to minimize the objective function of the ELDPP defined by (6), taking into account the equality constraints and the inequality constraints.

The cost function implemented in PSO is defined as:

$$F(x) = \alpha.[\sum_{i=1}^{ng}(a_i + b_i P_{gi} + c_i P_{gi}^2)] + (1-\alpha).[w.\sum_{i=1}^{ng}(a_i + b_i P_{gi} + c_i P_{gi}^2 + d_i e^{e_i P_{gi}})] \quad (11)$$

To minimize *F* is equivalent to getting a maximum fitness value in the searching process. The particle that has lower cost function should be assigned a larger fitness value. The objective of OPF has to be changed to the maximization of fitness to be used as follows:

$$fitness = f_{max}/_F \quad (12)$$

Where,

f_{max} : the maximum of $F_i(P_{gi} = P_{gi_{max}})$

The search of the optimal control vector is performed using into account the real power flow equation defined by (7) which present the system transmission losses (P_{loss}). These losses can be approximated in terms of *B* coefficients as [34]:

$$P_{loss} = \sum_{i=1}^{ng}\sum_{j=1}^{ng} P_{g_i}.B_{ij}.P_{g_j} \quad (13)$$

The B_{ij} coefficients are obtained from a power flow solution. These losses are introduced in the represented as a penalty vector given by:

$$pf = \left(1 - \frac{\partial P_{loss}}{\partial P_g}\right)^{-1} \quad (14)$$

In this method only the inequality constraints on active powers are handled in the cost function. The other inequality constraints are scheduled in the load flow process. Because the essence of this idea is that the inequality constraints are partitioned in two types of constraints, active constraints that affect directly the objective function are checked using the PSO-OPF procedure and the reactive constraints are updating using an efficient Newton Raphson Load flow (NR) procedure. Our objective is to search *(Pgi)* set in their admissible limits to achieve the optimization problem. At initialization phase, *(Pgi)* is selected randomly between Pgi_{min} and Pgi_{max}. After the search goal is achieved, or an allowable generation is attained by the PSO algorithm. It is required to performing a load flow solution in order to make fine adjustments on the optimum values obtained from the PSO procedure. This will provide updated voltages, angles and points out generators having exceeded reactive limits. to determining all reactive power of all generators and to determine active power that should be given by the slack generator taking into account the deferent reactive constraints. Examples of reactive constraints are the min and the max reactive rate of the generators buses and the min and max of the voltage levels of all buses. All these require a fast and robust load flow program with best convergence properties. The developed load flow process is based upon the NR algorithm using the optimal multiplier technique [35, 36].

The PSO algorithm applied to ELDPP can be described in the following steps.

Step 1: Input parameters of system, and specify the lower and upper boundaries of each control variable.

Step 2 : The particles are randomly generated between the maximum and minimum operating limits of the generators.

Step 3: Calculate the evaluation value of each particle using the objective function.

Step 4: Calculate the fitness value of objective function of each particle using (12). x_{ibest} is set as the *i th* particle"s initial position; x_{gbest} is set as the best one of $x_{ibest.}$ The current evolution is t =1.

Step 5: Initialize learning factors *c1*, *c2*, inertia weight *w* and the initial velocity *v1*.

Step 6: Modify the velocity *v* of each particle according to (9).

Step 7: Modify the position of each particle according to (10). If a particle violates its position limits in any dimension, set its position at the proper limits. Calculate each particle"s new fitness; if it is better than the previous *xgbest*, the current value is set to be *xgbest*.

Step 8: To each particles of the population, employ the Newton- Raphson method to calculate power flow and the transmission loss.

Step 9: Update the time counter t= t +1.

Step 10: If one of the stopping criteria is satisfied then go to step 11.

Otherwise go to step 6.

Step 11: The particle that generates the latest *pgbest* is the global optimum.

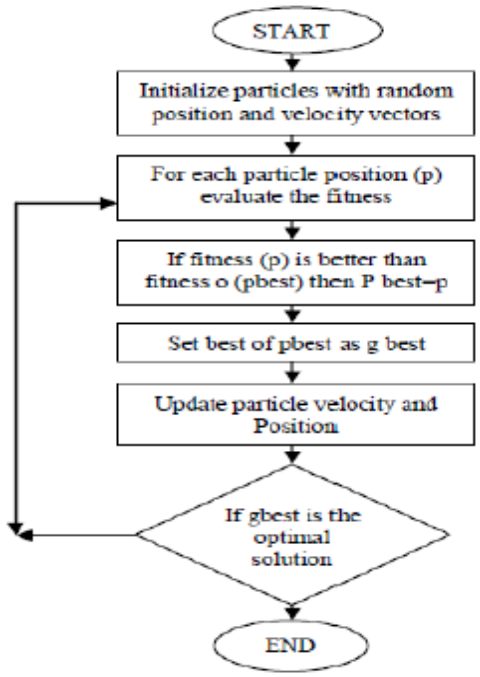

Fig. 2 : Flow chart for particle Swarm Optimization application to Economic load dispatch.

IV. APPLICATION STUDY

The IEEE 30- bus system with 6 generators is presented here. The total load was 283.4 MW.

Table.1

Power generation limits and cost coefficients for IEEE 30-bus system

Bus	$P_{g_{min}}$ (MW)	$P_{g_{max}}$ (MW)	a $\$/hr$	b $\$/MW.hr$	c $\$/MW^2.hr$
01	50.00	200.00	0	2.00	037.5
02	20.00	080.00	0	1.75	175.0
05	15.00	050.00	0	1.00	625.0
11	10.00	035.00	0	3.25	083.0
13	10.00	030.00	0	3.00	250.0
18	12.00	040.00	0	3.00	250.0

Upper and lower active power generating limits and the unit costs of all generators of the IEEE 30-bus test system are presented in Table 1.

The NOx emission characteristics of generators are grouped in Table 2. The emission control cost factor for 30-bus system was taken as 550.66 $/Ton.

Table.2

Pollution coefficients for IEEE-30 bus system

Bus	$\alpha.10^{-2}$	$\beta.10^{-4}$	$\Upsilon.10^{-6}$
1	4.091	-5.554	6.490
2	2.543	-6.047	5.638
5	4.258	-5.094	4.586
8	5.326	-3.550	3.380
11	4.258	-5.094	4.586
13	6.131	-5.555	5.151

The results including the generation cost, the emission level and power losses are shown in Table 3. This table gives the optimum generations for minimum total cost in three cases: minimum generation cost without using into account the emission level as the objective function (α=1), an equal influence of generation cost and pollution control in this function and at last a total minimum emission is taken as the objective of main concern (α=0). The active powers of the 6 generators as shown in this table are all in their allowable limits. We can observe that the total cost of generation and pollution control is the highest at the minimum emission level (α=0). As seen by the optimal results shown in the table 3, there is a trade off between the fuel cost minimum and emission level minimum. The difference in generation cost between these two cases (801,942 $/hr compared to 937,123 $/hr), in real power loss (9,428 MW compared to 3,749 MW) and in emission level (0,368 Ton/hr compared to 0.218 Ton/hr) clearly shows this trade-off.

Table 3

Results of minimum total cost for IEEE 30-bus system in three cases

Case I- (α=1)

Variable	Generation cost minimum
$P_{g_{01}}(MW)$	176,928
$P_{g_{02}}(MW)$	49,038
$P_{g_{05}}(MW)$	21,414
$P_{g_{08}}(MW)$	21,382
$P_{g_{11}}(MW)$	12,074
$P_{g_{13}}(MW)$	12,000
Generation cost($/hr)	801,942
Emission (ton/hr)	0,368
Total cost ($/hr)	1004,492
Power Loss (MW)	9,428

Case (II). (α=0.5)

Variable	Generation cost + Emission minimum
Pg01(MW)	129,984
Pg02(MW)	57,065
Pg05(MW)	25,471
Pg08(MW)	35,000
Pg11(MW)	22,148
Pg13(MW)	20,304
Generation cost ($/hr)	820,033
Emission (ton/h)	0,270
Total cost ($/h)	968,917
Power Loss (MW)	6,570

Case III. When α= 0,

Variable	Emission minimum
Pg01(MW)	66,760
Pg02(MW)	73,626
Pg05(MW)	50,000
Pg08(MW)	35,000
Pg11(MW)	30,000
Pg13(MW)	31,762
Generation cost ($/hr)	937,723
Emission (ton/h)	0,218
Total cost ($/h)	3,749
Power Loss (MW)	

Table 4.

Comparison between PSO and GA results for IEEE 30 bus system

a). for minimum generation cost

	PSO	GA
Generation cost ($/hr)	803.106	801.942
Emission (ton/hr)	0,3771	0.368
Total cost ($/hr)	1010.7	1004.5

b). for minimum generation cost with emission

	PSO	GA
Generation cost ($/hr)	824.988	820.033
Emission (ton/hr)	0.266	0.270
Total cost ($/hr)	971.4	968.9

c). For minimum Emission

	PSO	GA
Generation cost ($/hr)	943.1	937.12
Emission (ton/hr)	0.205	0.218
Total cost ($/hr)	1056.1	1056.9

PSO Based Combined Economic Emission Dispatch- In the proposed approach the minimum solution is obtained for PSO based combined economic emission dispatch with line flow constraints for IEEE 30 BUS system. The line flows in MVA of the best generation schedule for IEEE 30 BUS system were shown in table 5.

Table.5

Economic Generation Outputs of various evolutionary techniques and PSO

Output Power	GA	SA	EP	Proposed PSO
P_1	192.65	188.02	173.848	155.6326
P_2	48.912	47.45	49.998	20.0000
P_5	19.26	19.77	21.386	42.0000
P_8	10.58	13.40	22.630	35.0000
P_{11}	10.79	11.25	12.928	25.0000
P_{13}	12.24	14.09	12.000	12.0000
P_L	11.04	10.58	9.390	6.2326

Hence, the price penalty factor (Z) is determined as 2.3384 for IEEE 30 BUS system. The price penalty factor was computed up to 283.4 MW load demand. By incorporating price penalty factor approach, the total operating cost was obtained as 1624 $/hr for IEEE-30 BUS system.

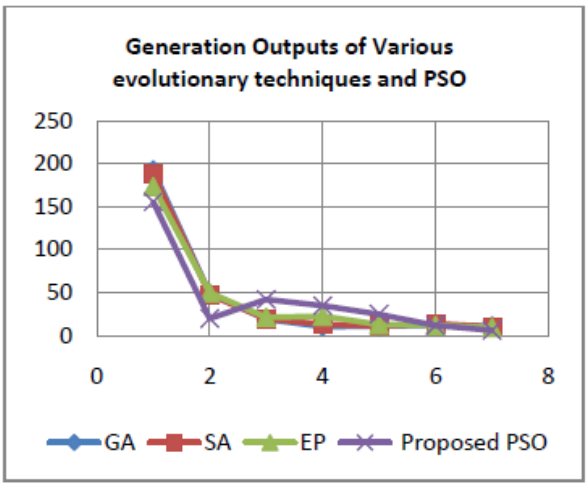

Fig . Comparison of Generation Outputs of various evolutionary techniques with Proposed PSO

To decrease the generation cost, one has to sacrifice some environmental constraint. The minimum total cost is at α=0.5 of the order of 968.917 $/h. The security constraints are also checked for voltage magnitudes, angles and branch flows. The voltage magnitudes and the angles are between their minimum and the maximum values. The results including the voltage magnitude of the different values of α (α=0, α=0.5, α=1) shown in (Fig. 1). The transmission lines loading do not exceed their upper limits. In addition, it is important to point out that this algorithm converges in an acceptable time. For this test system it was approximately 2

seconds. Table 4 shows a comparison between the PSO and Genetic Algorithm with real code [29]. The PSO is superior on GA in the two first cases: the generation cost minimum and the simultaneous minimization of fuel cost and emission cases, but in the case of the pure emission minimization GA gives slightly better values.

V. CONCLUSION

This paper introduces a Particle Swarm Optimization algorithm to solve the economic power dispatch of power system with pollution control. The fuel cost and emission are combined in a single function with a difference weighting factor. The main advantage of PSO over other modern heuristics is modelling flexibility, sure and fast convergence, less computational time than other heuristic methods. PSO requires only a few parameters to be tuned, which makes it attractive from an implementation viewpoint. The feasibility of the proposed algorithm is demonstrated on an IEEE 30-bus system. The results show that the proposed algorithm is applicable and effective in the solution of OPF problems that consider nonlinear characteristics of power systems with different objective functions. PSO can generate an efficiently high quality solution and with more stable convergence characteristics than Genetic Algorithm.

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Unified Control Strategy For DFIG Based Wind Power

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Abstract - This paper puts forth an effective control strategy for wind power plant to bring out additional transmission capacity and better means of maintaining system reliability when compared to already existing control techniques. Doubly Fed Induction Generator is taken for study. The rotor power of DFIG is the only controlling parameter taken to determine four current reference values using this single strategy. These references are fed to Rotor side and grid side current controllers which enables Torque, Grid side real and reactive power, as well as pitch angle control resulting in more prominent solution. This control strategy therefore relieves the need for switching between different controllers or reconfiguration of the hardware. This strategy also provides automatic voltage and frequency regulation for network. If the DFIG wind power unit is equipped with a battery, the proposed control enables islanded operation of DFIG wind power unit. The effectiveness and robustness of the proposed control strategy is studied through simulation carried out on detailed switched model of the system in the PSCAD/EMTDC version 4.2 software environment.

Keywords - *Unified strategy, doubly fed induction generator (DFIG), Voltage and frequency regulation, PSCAD/EMTDC version 4.2.*

I. INTRODUCTION

Renewable Energy resources are gaining in popularity and significance due to a variety of reasons with environmental concerns being the main driving force. Of such resources, wind turbine driven generators are by far the most prominent. Wind power has been integrated in to the power grid at high voltage transmission levels, medium voltage levels and also at distribution voltage levels. Each situation presents different challenges and they need to be studied and resolved for successful operation of the interconnected wind generation. Simulation studies have played a major role in almost all facets of wind power generation. PSCAD/EMTDC version 4.2 has been in the forefront of the wind power simulation technology and is the tool of choice of almost all leading wind power system vendors, utilities and researchers. For wind power integration PSCAD holds its application in:

- Design and analysis of grid Integration technology
- Wind turbine control optimization
- Design and verify the performance of the wind interconnection to ensure compliance with grid regulations and standards
    - Low voltage fault ride through requirements
    - Power quality issues including voltage flicker
- Design and verify the operation of protection equipment

II. EXISTING SYSTEM

Doubly Fed Induction machines using an AC-AC converter in the rotor circuit have long been a standard drive option for high power applications involving a limited speed range. The power converter need only be rated to handle the rotor power. Wind energy generation is regarded as a natural application for the DFIG system, since the speed range may be restricted. Most DFIGs use either a current fed DC Link converter or Cycloconverter in the rotor circuit. The rated speed settings, gearbox

ratios, and machine and converter ratings and the output power of the DFIG have been studied. The use of a current fed DC link converter has a number of disadvantages.

- High costs of the DC link
- The necessity of an extra commutation circuit for operation at synchronous speed
- Poor performance at low slip speeds.
- The converter draws rectangular current waveforms from the supply.

The problem at synchronous speed may be overcome by use of a Cycloconverter or Vector Controlled DFIGs. The disadvantages of the naturally commutated DC link and Cycloconverter can be overcome by the use of two PWM Voltage Fed Current regulated Inverters that are connected back-to-back in the rotor circuit. The characteristics of such a DFIG scheme with both Vector Controlled Converters are as follows:

- Operation below, above and through synchronous speed with the speed range restricted only by the rotor voltage ratings of the DFIG
- Operation at synchronous speed, with DC currents injected into the rotor with the inverter working in chopping mode
- Low distortion stator, rotor and supply currents independent control of the generator torque and rotor excitation
- Control of the displacement factor between the voltage and the current in the supply converter and hence control over the system power factor.

III. PROPOSED SYSTEM

Software intensive multidisciplinary systems are becoming so complicated that their procurement, specification, design, integration and test as well as their operation, use and maintenance are more and more challenging at each stage of the product lifecycle. In our work, we have stimulated wind power plant with efficient Unified Control technique, as shown in fig 1. Doubly Fed Induction Generator is used where stator is directly connected to grid and rotor is fed to AC-DC-AC back to back converter. In existing system different strategies are being used to control different parameters, which lead to switching losses. This seems to be an obstacle to extract maximum power from the sufficient availability of wind. Our work puts in single strategy with just four reference values to control the Torque, Stator Reactive Power, Grid-side Real and Reactive Power. The technique used is simple and does not require any deviation from present hardware configuration.

Based on the simulation results, it is proved that the proposed DFIG is capable of simultaneous capturing maximum power of wind energy with fluctuating wind speed and improving power quality, that are achieved by cancelling the most significant and troublesome harmonics of the utility grid. Dynamic Power Factor Correction and Reactive Power Control are the other two significant features of this technology.

The control strategy proposed is being simulated in subsystem converter module. Timed phase to ground fault is applied to the network near the load to analysis the performance of the system at fault condition and its recovering ability.

The grid is represented as source with necessary breaker arrangements. The opening and closing of breaker is provided by breaker logic model. Here initially breaker is in closed state when over current is detected it is set to open.

ADVANTAGES

- Fast, bump less transition from the grid connected mode to the islanded mode.
- Voltage/Frequency regulation for the network.
- Efficiency in extracting power from wind system is enhanced.
- Capable to function as a harmonic compensator, a load balancer and a load leveler.

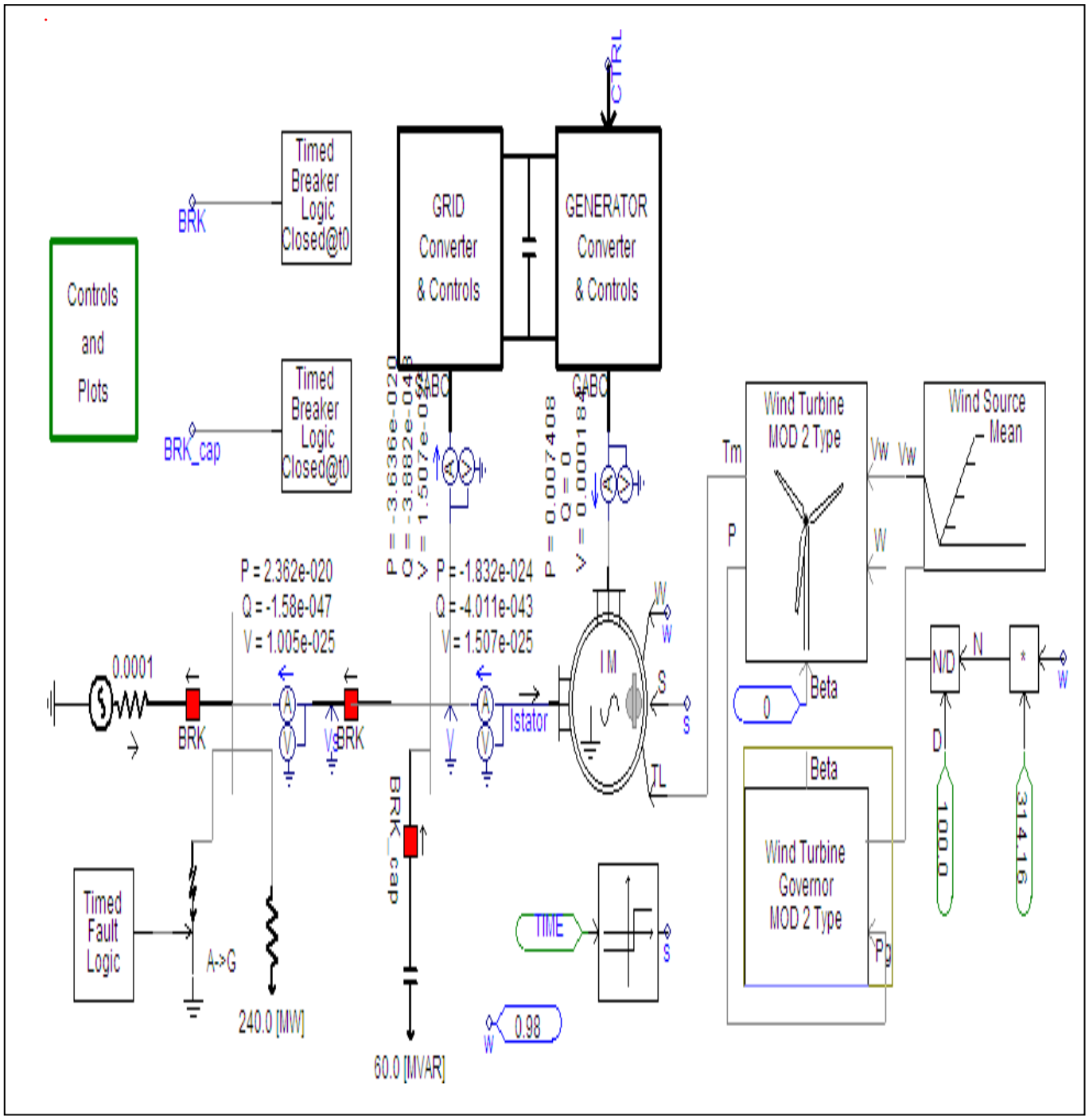

Fig. 1 : Simulink model of grid connected wind power system

IV. SIMULATION RESULTS AND DISCUSSION

To evaluate the effectiveness of the proposed control strategy, simulation studies are performed on a detailed switched model of the system in the PSCAD/EMTDC software environment.

A. Real power

The graph in Fig 2. describes the response of delivered real power from grid. Initial fluctuation represents the transient condition. Since fault is applied at 0.2 sec the power immediately reaches zero and remains null until breaker recovers at 0.8 sec. After few period of voltage swell, power reaches stability at 1.1 sec. This clearly tells that network regains its stability just within 0.2 seconds of breaker reclosure.

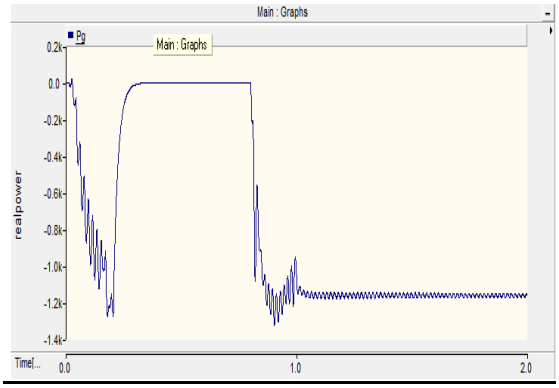

Fig. 2 : Real power response

B. Reactive power

The response of delivered reactive power from grid is being illustrated in Fig3. Initial fluctuation represents the transient condition. Since fault is applied at 0.2 sec the reactive power approaches zero and remains until breaker recovers at 0.8 sec. Then it tries to maintain value stable immediately but experiences voltage sag for milli seconds and power reaches stability at 1.2 sec. This clearly shows that, network regains its stability just within 0.3 seconds of breaker enclosures.

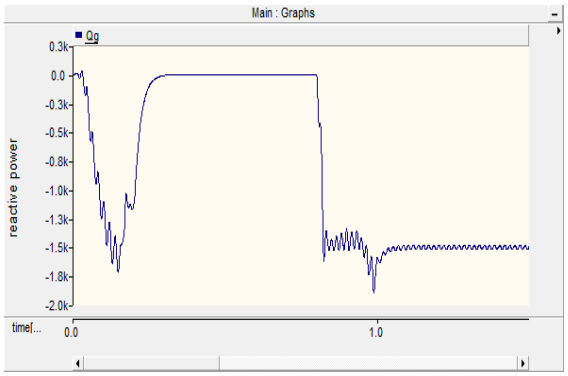

Fig. 3: Reactive power response

C. DC-link voltage

The power from stator is converted to DC and back to AC after being controlled. This voltage across DC-link capacitor is shown in fig 4. Initial dynamic behavior is predicted in the first time period of 0.2[sec]. Then when fault occurs breaker is simulated to open and voltage drops to zero. After fault is being cleared at 0.8 sec the current gets stable at 1 sec after a duration of 0.2 sec from breaker reclosure.

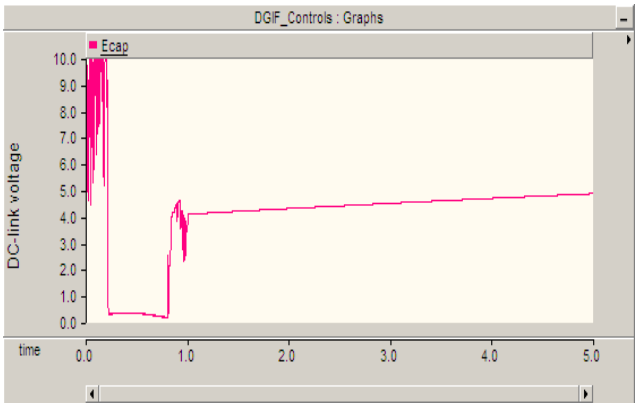

Fig. 4 : DC-Voltage link

D. Instantaneous current

The network is subjected to single phase ground fault at 0.2 sec in phase A. This trips the breaker immediately. The graph in fig 5 provides clear exposure of phase currents to fault and its response. The effected phase A has decrease in magnitude to larger extend. The other phases has light effect in magnitude, however once breaker opens instantaneous currents all three phase become zero. The effective control method makes the phase currents to obtain steady state at the instant of fault clearance.

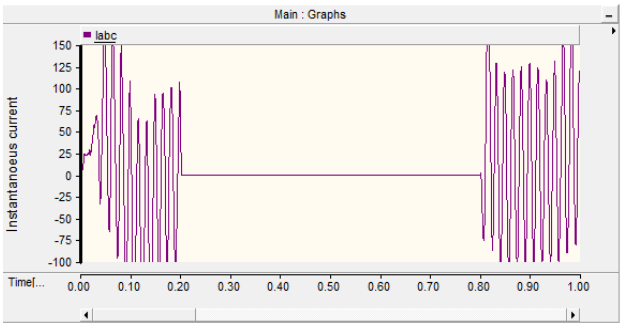

Fig 5 :Instantaneous current flow in distribution network

E. Rotor current

The graph in fig 6 indicates the response of rotor current. Initially after passing through converter it shows fluctuations due to dynamic characteristics. At 0.2 sec as breaker opens, current is pulled down to zero.

Then after recovery of fault it regains back to stable operation indicated in graph. The recovery time is very less which increases the efficiency

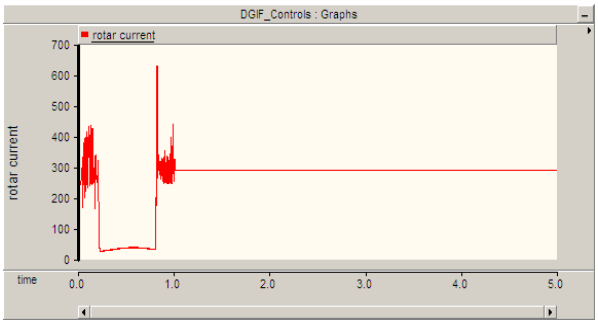

Fig. 6 : Rotorcurrrent

V. CONCLUSION

A multimode control strategy has been proposed for a Doubly Fed Induction Generator wind power unit. Under the proposed control strategy, the DFIG wind power unit can operate in the grid connected mode and preserves its characteristics. If the DFIG wind power unit is equipped with a battery, the proposed control also enables islanded operation of the DFIG wind power unit and features:

- Fast, bump less transition from the grid connected mode to the islanded mode
- Voltage/Frequency regulation for the network
- Operation with applied fault condition also studied
- Efficiency of tested network is found to be reasonably good.

The proposed control strategy employs a unified Controller for all of the aforementioned modes of operation and, therefore relieves the need for switching between different controllers or reconfiguration of the hardware.

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Multi-Patient ECG Monitoring System

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Abstract - An electrocardiogram (ECG) is bioelectric signal which records the heart's electrical activity versus time. ECG is an important diagnostic tool for accessing heart functions and diagnosing different heart abnormalities. This paper presents multi-patient ECG monitoring system, which acquires ECG signals from multiple patients and converts it into digital form using Data Acquisition System (DAQ). Data Acquisition System transmits these multiple signals into PC along single serial channel using standard serial protocol. In PC, using LabVIEW, we receive multiple ECG signals from patients and processing them for the purpose of display and monitor. The proposed system in this paper allows acquisition and monitoring of ECG signals from multiple patients in ICU using ECG acquisition, DAQ hardware, LabVIEW software and general purpose PC along single serial channel.

Keywords - *ECG acquisition, ECG monitoring system, ECG signal processing, ECG, LabVIEW, Serial transmission.*

I. INTRODUCTION

An electrocardiogram (ECG) is bioelectric signal which records electrical activity of heart. ECG is an important diagnostic tool for accessing heart functions and diagnosing different heart abnormalities. ECG signal consists of P wave, QRS complex and T wave as shown in Fig.1. The P wave represents depolarization of atria, QRS complex represents depolarization of ventricles and T wave represents repolarization of ventricles.

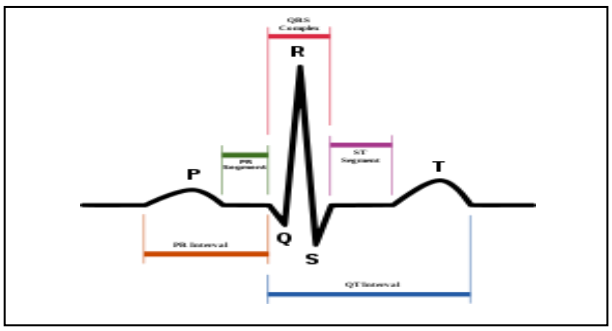

Fig. 1 : ECG signal [1]

The main objectives of this paper is to present

1. ECG acquisition system
2. Interfacing with PC
3. ECG display and monitoring.

II. ECG ACQUISITION SYSTEM

ECG signal is acquired from Lead-2 of patients using three electrodes, two for the differential inputs of the ECG instrumentation amplifiers and the third for ground. The ECG signals are typically in the millivolt range, and are hence susceptible to large amounts of interference, from a variety of sources like power line interference, baseline wandering due to patient movement and respiration, EMG interference due to muscular activity. So it is necessary to amplify the signal and remove noise from signal. Building blocks for ECG acquisition system are shown in Fig.2.

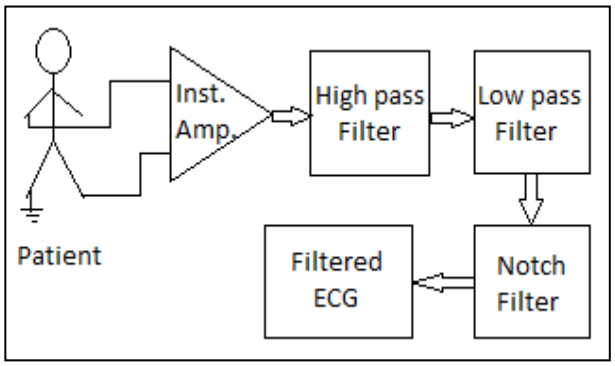

Fig. 2 : Block Diagram of ECG acquisition system

Instrumentation Amplifier:

It differentiates the signal from RA & LL and removes the common signal. Deference of them gives the electric activity of the heart called ECG. It is used mainly to remove the common mode signal and amplify the signal.

High pass Filter:

High pass filter is used in order to remove low frequency changes of the baseline wandering due to

respiration and movement of the patient. It is 4th order Butterworth high pass filter with cutoff frequency of 0.5HZ.

Low pass Filter:

Low pass filter is used to remove a very high frequency noise. It has mainly EMG interference due to muscular activity. It is 4th order Butterworth low pass filter with cutoff frequency of 100 HZ.

Notch Filter:

A 50 Hz notch filter is used to remove the power line interference.

Summing Amplifier:

The signal must be brought into the range of zero to five volts to enable the analog to digital converter to perform analysis on it. After summing amplifier, the base line of the ECG signal has been brought to an offset of 1 or 2 volt depending upon how much DC voltage has been summed with the signal.

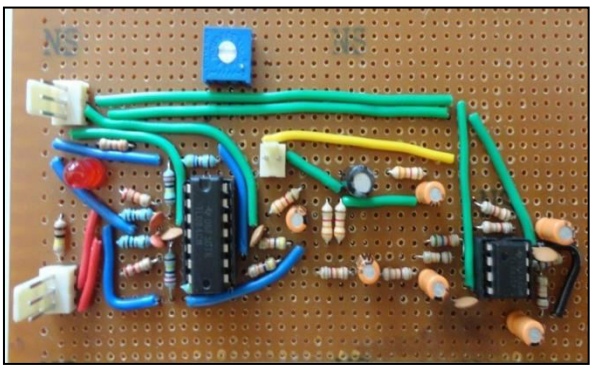

Fig. 3 : ECG acquisition system

III. MULTICHANNEL DATA ACQUISITION SYSTEM

DAQ (Data Acquisition) can be defined as the process of acquiring a real-world signal, such as a temperature, pressure, voltage, current or any other signal into the computer, for processing, analysis, storage or other data handling. Analog data is usually acquired and renewed into the digital form for the principle of processing, transmission and display [2]. Four different types of analog signals are applied to DAQ, which converts analog signal into digital signal and is able to transmit all the four signals into pc without distortion.

The whole DAQ system consists of microcontroller based DAQ and personal computer with LabVIEW software and drivers. The block diagram for system is shown in Fig.4.

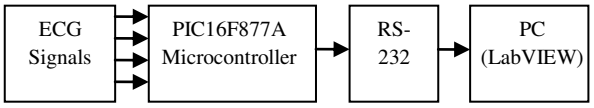

Fig. 4 : Block Diagram of Multichannel DAQ

ECG signals from patients are in analog form. To be interface with pc, they must be into digital form. This DAQ system uses PIC16F877A microcontroller which has inbuilt 8 channel 10 bit ADC. This inbuilt ADC samples the analog signal and converts analog signal into digital signal. Once the digital data corresponding to analog signal is available, pic microcontroller transmits this digital data to pc via serial channel using standard serial protocol.

In serial communication, the data is sent as one bit at a time. The interfacing of PIC microcontroller (PIC16F877A) with a computer is done via serial port using RS232. The microcontroller communicates with the PC through the serial interface RS232. A MAX232 is used to convert voltage levels from the RS232 standard (+-12V) to TTL levels (+-5V) that the microcontroller uses and baud rate of 9600 bps is set for serial transmission. Multiple analog signals are digitized and transmitted to pc simultaneously and on other side in pc; receive multiple signals simultaneously in LabVIEW. GPB mounted DAQ system is shown in Fig.5.

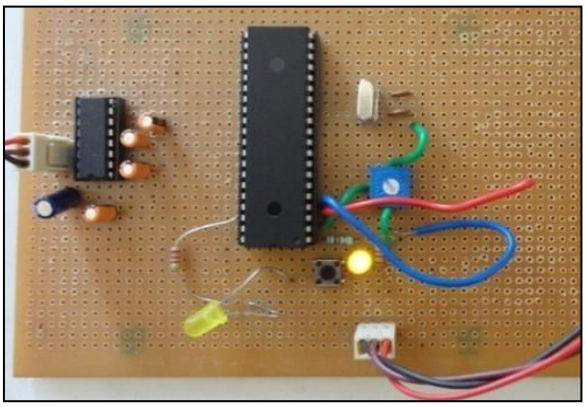

Fig. 5 : Multichannel DAQ

By using this DAQ system, one can be able to interface maximum 8 ECG signals from different patients with microcontroller and able to display and monitor all the signals simultaneously.

IV. ECG DISPLAY AND MONITORING

The ECG signals from multiple patients are transmitted by PIC controller via single serial channel and are received in LabVIEW. In LabVIEW, GUI is

designed to receive multiple ECG signals via serial port and differentiate various ECG signals from multiple patients sent along single channel.

Once ECG signals are brought into PC, we filter the ECG signals to further remove the noise. Here, we use digital IIR filter in LabVIEW to remove noise from ECG. After filtering the ECG signals we have to find the heart rate for the purpose of patient monitoring. To find heart rate, we detect QRS peak in ECG signal and find time interval between consecutive QRS peak. Based on this time interval between two peaks, the heart rate of patient is calculated. After calculating heart rate, ECG from multiple patients and their corresponding heart rate are displayed in GUI using chart recorder. In this way, ECG signals from multiple patients are displayed and monitored.

V. RESULTS

ECG signals from four different patients are acquired and are successfully displayed and monitored using this system. Multi-patient ECG Display and monitoring GUI for four patients is shown in Fig.6.

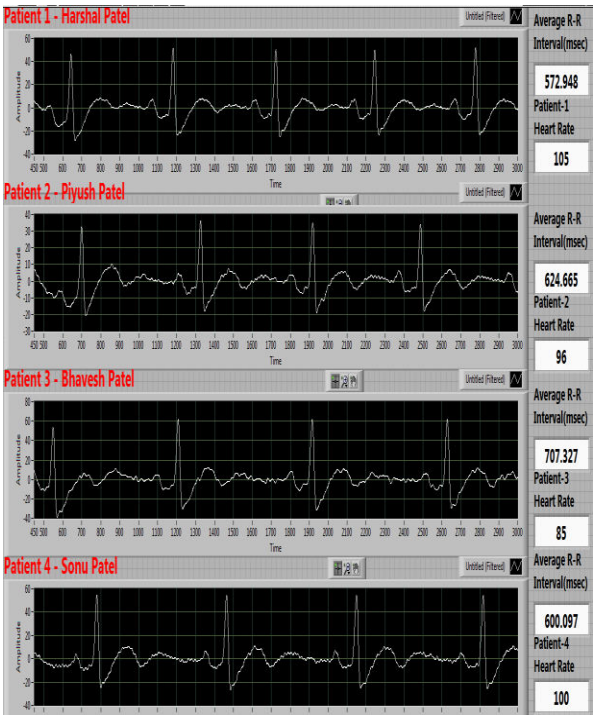

Fig. 6 : Multi-patient ECG monitoring

VI. CONCLUSION

By using this system, one can be able to successfully display and monitoring multiple ECG signals from maximum 8 patients using single serial channel and minimize requirement of multiple channels for multiple patients.

ACKNOWLEGEMENT

I would like to express my gratitude to my guide, Prof. Mitul Patel who showed confidence in me, encouraged and supported me throughout my work. It gives me immense pleasure to remember the ocean of guidance, support and encouragement from innumerable sources.

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Breath Odor Detection Based on Electronic Olfaction For Asthma Classification

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Abstract - This paper outlines the development of the prototype able to classify the Asthma level. In recent years, there have been increasing concerns about the applications of breath analysis in medicine and clinical pathology both as a diagnostic tool and as a way to monitor the progress of therapies. Compared with other traditional methods, such as blood and urine test, breath analysis is noninvasive, real time, and least harmless to not only the subjects, but also the personnel, who collect the samples. The measurement of breath air is usually performed by gas chromatography (GC) or electronic nose (e-nose). GC is very accurate, but is expensive and not portable, its sampling and assaying processes are complicated and time consuming (about 1 h for one sample), and its results require expert interpretation. Recently, e-noses have gradually been used in medicine for the diagnosis of renal disease, diabetes, lung cancer, and asthma.

Electronic olfaction is the term associated with E-nose used to describe the system which consists of of electronic chemical sensors with partial electivity and an appropriate pattern recognition system, capable of recognizing simple and complex odors.

Keywords - *E-nose, LabVIEW.*

I. INTRODUCTION

Disease detection by medical diagnosis has developed rapidly in recent years. Blood and urine are most commonly used in diagnosis as compared to breath. In contrast to blood and urine, breath analysis is easy, specific and highly qualitative. Breath analysis is intended for diagnosis of clinical manifestations of airway inflammations, metabolic disorders and gastroenteric diseases. Breath had analysis by new high quality technical instrument. Its analytical results are qualitative and quantitative as compared to analysis of blood and urine.

Human breath is largely composed of oxygen, carbon dioxide, water vapor, nitric oxide, and numerous volatile organize compounds (VOCs). The type and number of the VOCs in the breath of any particular individual will vary, but there is nonetheless a comparatively small common core of breath, which are present in all humans. The molecules in an Individual's breath may be exogenous or endogenous. Exogenous molecules are those that have been inhaled or ingested from the environment or other sources, such as air or food, and hence, no diagnostic value. Endogenous molecules are produced by metabolic processes and partition from blood via the alveolar pulmonary membrane into the alveolar air. These endogenous molecules are present in breath relative to their types, concentrations, volatilities, lipid solubility, and rates of diffusion as they circulate in the blood and cross the alveolar membrane. Changes in the concentration of the molecules in VOCs could suggest various diseases or at least changes in the metabolism. Table I summarizes the typical compositions found in the endogenous breath of healthy persons.

TABLE I

TYPICAL COMPOSITION FROM THE ENDOGENOUS BREATH OF THE HEALTHY PERSONS

Concentration(v/v)	Molecule
Percentage	Oxygen, water, carbon dioxide
Parts-per-million	Acetone, carbon monoxide, methane, hydrogen, isoprene, benzenemethanol
	Formaldehyde, acetaldehyde, 1-pentane, ethane, ethylene, other hydrocarbons, nitric oxide, carbon disulfide, methanol,

	carbonyl sulfide, benzene, naphthalene, benzothiazole, ethane, acetic aide

TABLE II

BREATH COMPOUNDS AND ASSOCIATED CONDITIONS

Breath compounds	Associated Condition
Acetone	Diabetes
Ammonia	Renal disease
Nitric oxide	Asthmatic inflammation

Some molecules, such as nitric oxide, isoprene, pentane, benzene, acetone, and ammonia may indicate specific pathologies [7-9]. To take a few examples, nitric oxide can be measured as an indicator of asthma or other conditions characterized by airway inflammation [10]. Acetone has been found to be more abundant in the breath of diabetics [11]. Ammonia is significantly elevated in patients with renal disease [12]. Table II lists some breath compounds and the conditions that research has found to be associated with them. The compounds and conditions listed in Tables I and II were the focus of the work being described.

In this paper, all contributions have been concerned particularly for Diagnosis and the classification of Asthma level.

II. BREATH DETECTION UNITS

The proposed system operates in three phases (see Fig.1), gas collection, sampling, and data analysis, with a subject first breathing into a Tedlar gas sampling bag. This gas is then injected into a chamber containing a sensor array, where a measurement circuit measures the interaction between the breath and the array. The signals are then filtered and amplified and sent to computer for further analysis.

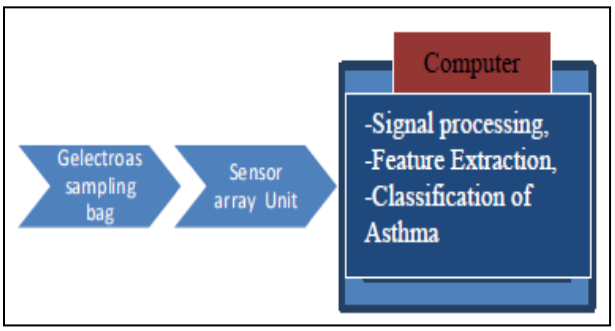


Fig. 1: Gas detection System

2.1 Gas Sampling Bag

Breath can be applied to the sensor by the two ways. Patient can be allowed to exhale breath on Sensor unit or the stored sample of the breath from the Patient is being to apply to the sensor unit.Subject's breath is collected using a 600 mL Tedlar gas sampling bag (A), an airtight box (B) filled with disposable hygroscopic material to absorb the water vapor from the breath, and the last component, a disposable mouthpiece (C)

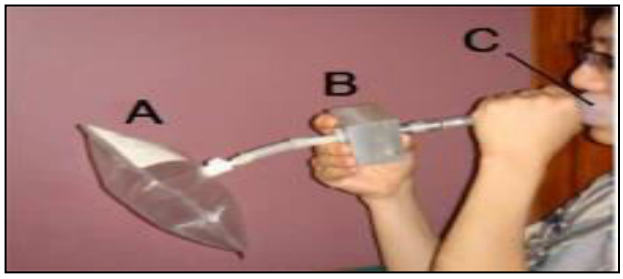


Fig. 2: Gas sampling bag

The hygroscopic material is silica gel. It is stable and only reacts with several components, such as fluoride, strong bases, and oxidizers. None of them is involved in the breath components.

2.2 TGS Figaro sensor

The models tested were Figaro TGS 2201 sensor. The sensor responds in presence of Nitrous oxide from patient's breath which is the biomarker for Asthma detection. When Nitrous oxide is present an oxido-reduction reaction occurs on the sensing element and the surface resistance changes. This produces an output signal 0 to 5 volts that corresponds to the gas concentration. Table III shows the TGS sensors used for associated condition.

TABLE III

TYPES OF SENSORS AND CORRESPONDING SENSETIVE GAS:

Sensors	Gas	Sensitivities (ppm)
TGS2201	NO or NO_2	0.1-10
TGS826	NH_3	30-300
TGS821	H_2	100-1000

2.3 The sensor Response

The response of e-nose sensors to odorants is generally regarded as a first order time response. The first stage in odor analysis is to flush a reference gas

through the sensor to obtain a baseline.

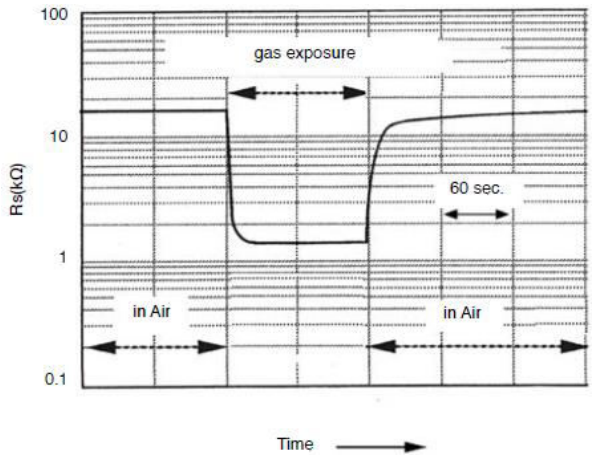


Fig. 3: TGS Figaro sensor response

The sensor is exposed to the odorant, which causes changes in its output signal until the sensor reaches steady-state. The odorant is finally flushed out of the sensor using the reference gas and the sensor returns back to its baseline as shown.

III. DEVELOPMENT OF SYSTEM

The models tested were Figaro TGS 2201 sensor. When a gas is present an oxido-reduction reaction occurs on the sensing element and the surface resistance changes. This produces an output signal 0 to 5 volts that corresponds to the gas concentration. This signal is connected to the analog in pins AN0 – AN7 of the PIC microcontroller. The sensors coil needs to get heated up in able to function. To get sufficient current to heat up the coil it is not enough to connect it directly to a digital output of the microprocessor. Instead the current needs to be amplified with bipolar transistors.

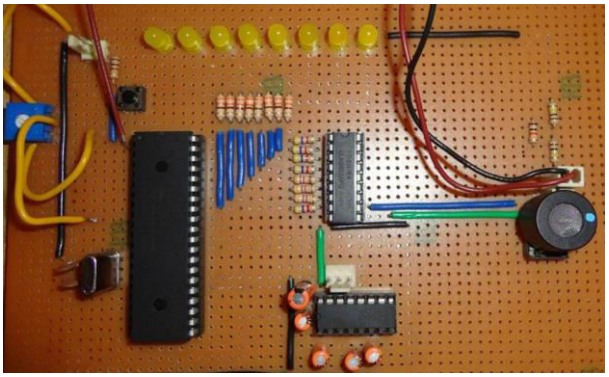


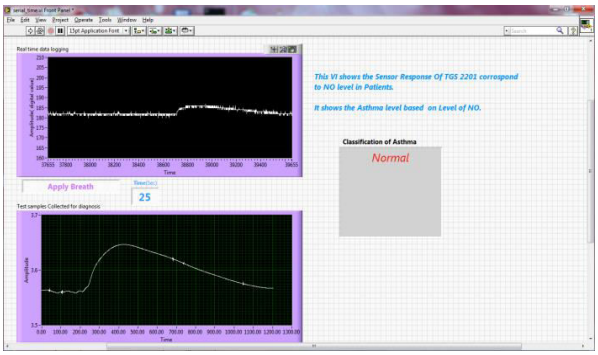
Fig. 4 : Hardware Unit

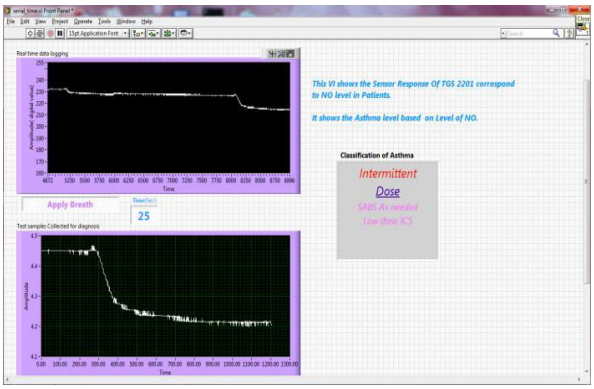
There are different ways of doing this. With a NPN transistor pin 5 is connected to ground or with a PNP transistor pin 5 is connected to 5 volts. With the integrated circuit ULN2803 it is possible to connect up to 8 sensors on a single chip. The ULN2803 is an 8 Channel Darlington Array mostly popular in stepper motor applications. But it obviously serves well for driving gas sensors also. Its outputs are inverted so when input I1, I2, …, I8 is high its corresponding output O1, O2, …, O8 will be low which will produce a current through the coil because the other side is connected to 5V. When the input is low the output becomes high and there will be no current through the coil as both sides of it will be 5V, which means that the sensor is turned OFF.

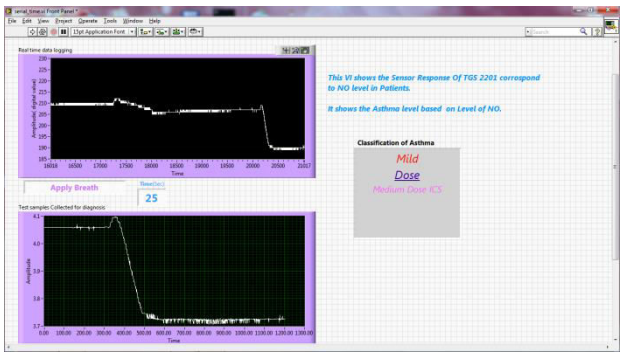
IV. SOFTWARE DEVELOPMENT

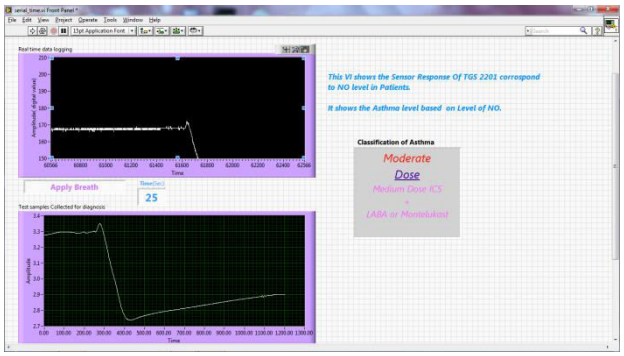
Virtual Instrument Software Architecture (VISA) is a standard interface library comprising RS-232 and other protocols. VISA provides the programming interface between the hardware and development environments such as LabVIEW. LabVIEW comes with interactive tools and configuration utilities for VISA. However it is very easy to make mistakes about how to use this library. Reception of a continuous serial data flow with unknown length demands much more than just receiving a data stream with a known length.

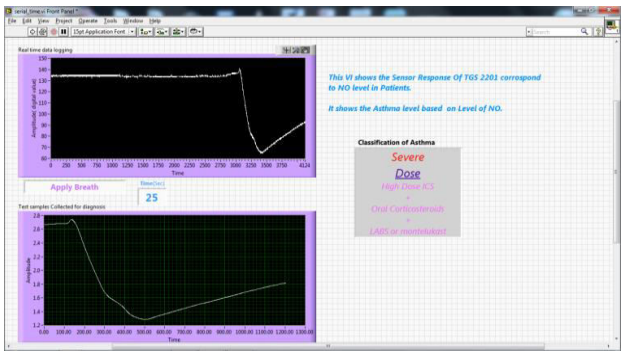
The total time duration of the test is of 25 seconds. Initial 15 seconds are spent to get a steady state level of the TGS sensor. While the sensor accommodates with the environment, the timer clearly displays time elapsed. After 15th second, the message box displays “Apply Breath” and the test being made for another 10 seconds.











After completion of 25 seconds, the VI filters the signal using wavelet de-noising and calibrates the results using peak & valley detection of the sensor response. The ultimate change is calculated and according to the change measured with sensor, the system gives results of severity of asthma with the drug dosage given by the asthmatic guidelines [13-15].

V. CONCLUSION

By using TGS 2201 Sensor, the nitrous oxide is detected. In LabVIEW with the help of VISA, the Analog output of the sensor is serially transmitted to PC. After processing the signal and extracting the features, Classification of Asthma level is achieved weather it is mild, moderate, intermittent and severe Asthma.

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Core Taste Identification and Water Quality Assessment by an Artificial Taste Sensor Based on Conductometry

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Abstract - This paper presents a method for identification of basic tastes, i.e. sweet, sour, bitter and salty with the help of electronic tongue and for assessing the quality of water. The artificial sensor works on the basis of conductometric technique and having two electrodes. This technique determines the level of current flow as a function of voltage when polarization of ions occurs around the electrode. This measured current is a function of different chemical composition and hence can be used for the identification of different taste, as different taste having different chemical composition and quality of water. The main objective of the present work is to test samples from four different tastes and various types of water with the help of an artificial taste sensor and analyzing the output current obtained from different samples in time domain.

Keywords - *An artificial taste sensor, Basic Test, Conductometry, Electrode.*

I. INTRODUCTION

An artificial taste sensor is also called as an electronic tongue. Electronic taste instruments have been developed and optimized to answer some of these issues: reduces human sensory test panels, precise measurement of taste, requires small sample volume, decreased measurement time, small size of sensor, reproducibility, easily operated by unskilled personnel. An electronic tongue is a sensor that works on the liquid samples. The responses of the sensor are not specific. The collective response of the taste sensor varies from solution to solution due to the presence of different compounds and ions. An artificial taste sensor, in general, makes use of this collective response, and various electrochemical methods have been exploited for such analysis. Potentiometry, Voltammetry, and conductometry are some of the measurement techniques that have been used successfully in this kind of sensors for different applications, such as classification of wine, assessment of fat content of milk, quality evaluation of several beverages like tea, beer, and juice, water quality [1], and other food stuffs like tomatoes [2]. This can also be used in pharmaceuticals to identify the taste of medicine [3].

The electroanalytical technique called the conductometry, which is one of the oldest and in many ways simplest among the other electroanalytical techniques. This technique is based on the measurement of electrolytic conductance. An application of electrical potential across the solution of an electrolyte involves the transfer of mass and charge from one part of the solution to the other. A transport property of great significance, which can be easily measured, is the conductance. The conducting ability of electrolytic solutions provides a direct proof of the existence of ions in solutions. The experimental determinations of the conducting properties of electrolytic solutions are very important.

The main objective of the present work is to test samples from four different tastes and different water samples with the help of an artificial taste sensor and analyzing the output current obtained from different solution in time domain. It can also be used for food quality assessment. The procedure when running measurements with an artificial taste sensor set up seen from the user's viewpoint is often straightforward. Take a sample of the requested liquid, put it in contact with an artificial taste sensor and receive the response. Behind this simplified process are both the operational principle of an artificial taste sensor and the data acquisition.

II. AN ARITIFICIAL TASTE SENSOR SET UP

The sensor consists of two copper electrodes. A potential is applied at one electrode and the resulting current through the sample is measured. When a voltage is applied, an electrochemical redox reaction occurs at the electrodes surface and gives rise to the measured current. All particles in the measured sample that are

redox reactive below the applied voltage will contribute to the response. The method used is pulse conductometry which indicates that the input waveform is formed by pulses of some amplitude. By using pulses of different amplitude, the sensitivity can be increased and the discrimination between samples will be improved. Depending on the sample's chemical content, the amount of particles contributing to the current will differ. The functional block diagram of the present system is as follows:

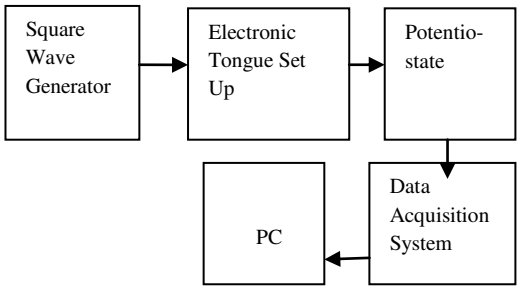

Fig. 1: Functional block diagram of the an artificial taste sensor

The 555 timer connected as astable multivibrator can be used to produce a square wave output. The artificial taste sensor system consists of two electrodes as sensor. Here, two copper plates are used to make an electrochemical cell. This set up is put in contact with the requested liquid. A potentiostate measures the potential difference between the two electrodes. The basic potentiostate consists of two parts, I/E Converter and DC Level Offset [4]. The data acquisition system establishes the communication between the sensor and data processing system. The configuration of the Data Acquisition System was implemented MATLAB environment. Note, that it is not identical to the functionality of the human tongue [5].

III. SAMPLES DETAILS AND PREPARATION

Four different taste samples such as Bitter, Salt, Sour and Sweet have been taken for this study. Kitchen salt (NaCl) is used as salty sample. Similarly, lemon juice is used as sour, Sugar is used for sweet taste and bitter juice from some food stuffs is used for bitter taste. For preparing the salty sample, 5gm of salt is dissolved in 20 ml distilled water. Sweet sample is made by dissolving 5 gm of sugar in 20 ml distilled water. Same way sour and bitter samples are prepared by mixing lemon juice and juice of bitter food stuff. Samples from different water types have been taken for water quality assessment. Experiments are performed on the distilled water, tap water and purified water (15 ml). Here the input is taken as voltage and output is as current. By giving the same input for each sample, the responses from the sensor are observed [6].

IV. RESULTS AND DISCUSSION

Experimental data collected from the setup is plotted as the response of an artificial taste sensor for the different sample as mentioned above. Response of the system for all different samples is quite same. But their amplitudes are different. It is observed that the time domain response of the above mentioned different samples is different, i.e. the maximum and minimum peak values of the different responses are different (Table 1 and Table 2). So with the response of an artificial taste sensor setup for different sample may possible to distinguish them from each other.

Table 1: Max and min peak values of different taste samples

Sr. No.	Taste	Current	
		Maximum value	Minimum value
1	Salty	2.9693	-0.7084
2	Sweet	0.0846	-5.9314e-04
3	Sour	2.3405	-0.1398
4	Bitter	1.2822	-7.3915e-04

From table-1, it is observed that the response for the salty sample has the highest peak value, and sweet sample has the lowest.

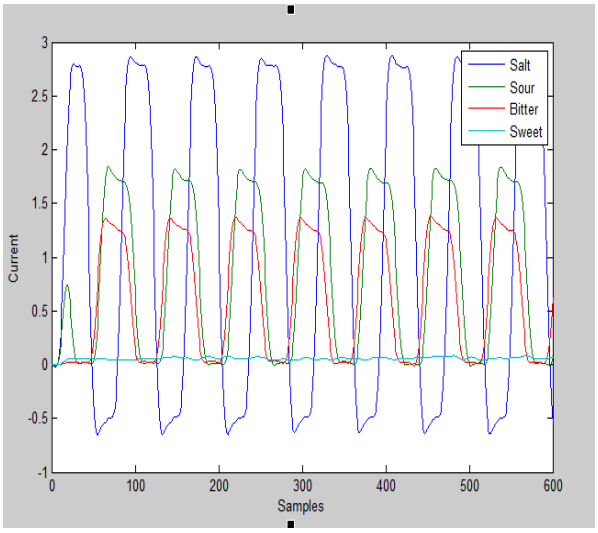

Fig. 2 : Correlation of responses of different taste samples

Table 2: Max and min peak values of different water samples

Sr. No.	Water	Current	
		Maximum value	Minimum value
1	Distilled water	0.0006	-0.0891
2	Tap water	1.3017	-0.0675
3	Purified water	0.0627	-4.0370e-04

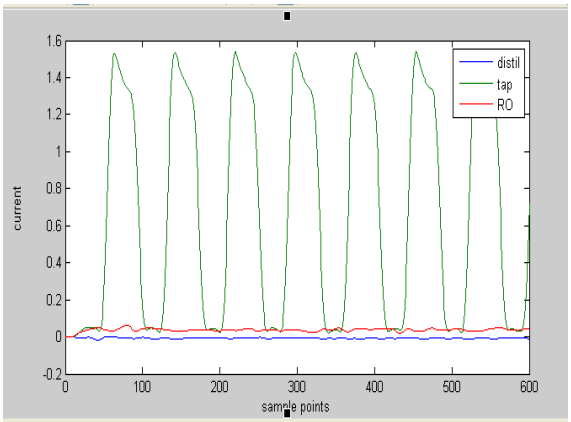

Fig. 3 : Correlation of responses of different water samples

V. CONCLUSION

In this paper, an artificial taste sensor system based on conductometry for taste evaluation and water quality has been presented. The best results have been obtained by taking the value of each response by set-up for different samples. This can be concluded that different samples have different current carrying capacities. This is because of current carrying ions present in the solution to be tested. The salty sample is found with a highest current and sweet sample with lowest current through the liquid during the experiments. The tap water sample is found with highest current through the liquid sample during experiments. Hence, this artificial taste sensor approach is helpful in taste identification of core tastes and water quality assessment.

VI. ACKNOLEDGEMENT

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Evaluation of Bag of Visual Words for Category Level Object Recognition

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Abstract - Object recognition in a large scale collection of images has become an important application in machine vision. The recent advances in the object or image recognition for classification of objects shows that Bag-of-visual words approach is a better method for image classification problems. In this work, the effect of different possible parameters and performance evaluation of Bag of visual words approach in terms of their recognition performance such as Accuracy rate, Precision and F1 measure using 8 different classes of real world datasets that are commonly used in restaurant applications is explored. The system presented here is based on visual vocabulary. Features are extracted, clustered, trained and evaluated on an image database of 1600 images of different categories. To validate the obtained results,a performance evaluation on vehicle datasetsunder SURF and SIFT descriptors with K-means and K-medoid clustering and KNN classifier has been made. Among these SURF K-means performs better.

Keywords - *Bag-of-visual words; SURF; SIFT; K-means; K-medoid; KNN classifier.*

I. INTRODUCTION

Object recognition in computer vision is the task of finding a given object in an image or video sequence. Every day a multitude of familiar and novel objects are recognized, though these objects may vary somewhat in form, colour and texture and so on. Theultimate goal of object recognition is validation, detection, category recognition, scene or context recognition and also activity recognition.

Object Recognition using Bag of Features (BoF) has gained enormous popularity in image classification techniques. It has been shown that Bag of Words (BoW)[1, 2, 3, 4, 5] approach provides several advantages with acceptable recognition performance, faster run time and reduced storage.Similar techniques are implemented in text information retrieval and text categorization.The main idea in this algorithm is that the descriptors are quantized to form a visual word dictionary called codebook with the help of different clustering algorithms. The BoW model allows a dictionary-based modelling. Computer vision researchers use a similar idea for image representation which is called the Bag of Feature (BoF) model. Each vector in the codebook being a visual word serves as the basis for indexing the images. The main task ofBag of Feature (BoF) is to classify a given image in to one of the pre-determined objects based on the trained classes of objects and to increase detection rate of images by adapting different descriptors, clustering algorithms and classifiers. Here hard clustering algorithms like K-means and K-medoidare used. The performance of the algorithms implemented is compared by varying the dictionary size.

II. BAG- OF- VISUAL WORDS ALGORITHM

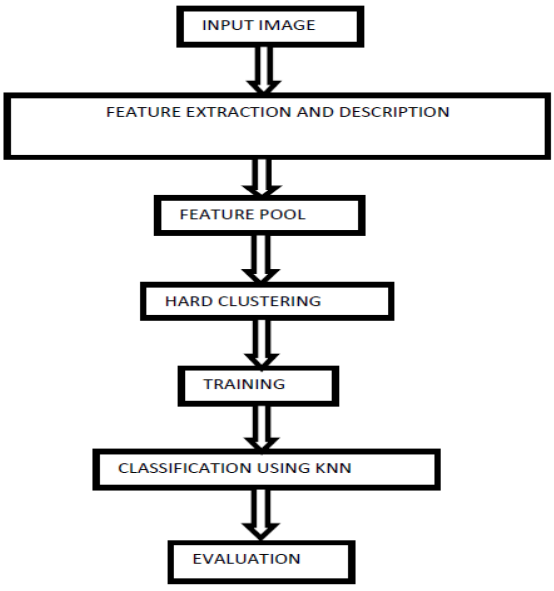

Fig. 1 : Schematic of Bag- of- Visual Words algorithm

In Bag of Words model features are extracted using detectors or dense sampling and descriptors are calculated at each and every local feature extracted. Thefeaturesextracted from the images should be easily detected under changes in pose,illumination and should be distinctive. There should be many features per object. After feature extraction,features are hard clustered bydata clustering techniques like K-means and K-medoid. After clustering a visual vocabulary is obtained with predefined number of visual words. In training phase, the input vectors from the feature pool are assigned to one or more classes. The decision rule divides input space into decision regions separated by decision boundaries and histogram is built up. In testing phase, for the test data point, the k closest points from training data is found and classification is done using KNN classifier. Figure.1 shows the schematic of Bag-of- Visual Words algorithm.

III. FEATURE EXTRACTION

Recognition is a basis issue for robots, and featureextraction is the very important part of this process. Highquality of feature extraction will play a crucial role on the results of recognition.Features are generally a random collection of points in an image or it may be a collection of distinctive points in an image like blobs and corners which are likely to be repeatable. For local feature detection, classic detectors include Harris detector [6] and its extension [7], maximally stable external region detector [8], affine invariant salient region detector [9]. For local feature description, local descriptors such as Haar descriptor [10], scale-invariant feature transform (SIFT) descriptor [11], gradient location and orientation histogram (GLOH) descriptor [12], rotation-invariant feature transform (RIFT) descriptor [13], shape context [14], histogram of gradients (HOG) descriptor [15] and speeded up robust feature descriptor (SURF) [16] are usually used.Inthis work Harris detector with SIFT (128 D) descriptor and Hessian detector with SURF (64 D) descriptor are used.

A. SIFT descriptor using Harris detector

The major stages in computations include four steps. (1) Identifying key points (Harris detector) (2) key point localisation (3) orientation assignment (4) key point descriptor computation (SIFT).

The Harris detector is a scale, rotation, and translation invariant interest point detection algorithm that has also shown to be robust to illumination variations, camera noise and viewpoint changes.The Harris detector is based on the second moment matrix. The second moment matrix given in equation (1), also called the auto-correlation matrix,defined for each pointp is often used for feature detection or for describing local image structure.

$$C = \begin{bmatrix} \sum L_x^2(x,y) & \sum L_x L_y(x,y) \\ \sum Lx\ Ly\ (x,y) & \sum L_y^2(x,y) \end{bmatrix} \quad (1)$$

Here, Lx and Ly denote the respective x and y gradient magnitude images, and the summation is taken over all points in a neighbourhood of point p. Thematrix C can be seen as a covariance matrix of the Gradient magnitude within a neighbourhood. It is real and symmetric, and so it can be decomposed into its principal components, with Eigenvalues λ_1 and λ_2. Harris noted the following in regions of constant intensity, $\lambda 1 = \lambda 2 = 0$.In regions with very little intensity variation, both $\lambda 1$and $\lambda 2$ will be small.For an edge region, the variation in one direction will be strong, and the variation in the otherdirection will be weak. Therefore, $\lambda 1$ will be large, and $\lambda 2$will be small. For a corner region, there will be strong variations in both directions and so both $\lambda 1$and $\lambda 2$willexceed some threshold value.

Key point localisation attempts to remove unstable key points from the final list by finding those that are poorly localised on an edge or corner.Orientation assignment aims to assign a consistent orientation to the key points based on local image properties. The key point descriptor can then be represented relative to this orientation, achieving invariance to rotation. The gradient magnitude, *m,* orientation(x,y) are given by the equations (2) and (3).

$$m(x,y) = \sqrt{\big(L(x+1,y) - L(x-1,y)\big)^2 + \big(L(x,y+1) - L(x,y-1)\big)^2} \quad (2)$$

$$\mu(x,y) = \big((L(x,y+1) - L(x,y-1))/(L(x+1,y) - L(x-1,y))\big) \quad (3)$$

Further the local image gradientsare measured in the region around each key point. These aretransformed into a representation that allows for significant levels of local shape distortion and change in illumination. The local gradient data is also used to create key point descriptors. The gradient information is rotated to line up with the orientation of the key point. These data are then used to create a set of histograms over a window centered on the key point. Key point descriptors typically use a set of 16 histograms, aligned in a 4×4 grid, each with 8 orientation bins, one for each of the main compass directions and one for each of the mid-points of these directions. This process results in a feature vector, containing 128 elements.

B. *SURF descriptor using Hessian detector*

SURF [16] outperforms or approximates previously proposed schemes with respect to repeatability, distinctiveness and robustness and it can be computed and compared faster. It is achieved by relying on integral images for image convolutions and by building strengths on leading detectors (Hessian detector) and descriptors.

The major stages in computations include:

(1) Interest point detection which involves computing integral images and Hessian matrix- based interest points.

(2) Scale space representation.

(3) Interest point localization.

Integral images allows for fast computation of box type convolution filters. The entry of an integral image $I_{\epsilon(x)}$ at a location x = $(x,y)^T$ given by equation (4) represents the sum of all pixels in the input image I within a rectangular region formed by the originand *x.*

$$I_{\epsilon(x)} = \sum_{i=0}^{i\leq x} \sum_{j=0}^{j\leq y} I(i,j) \quad (4)$$

Hessian matrix- based interest points are used for its good performance and accuracy.Given a point *x=(x,y)* in an image I, the Hessian matrix H*(x,ρ)* in *x* and scale *ρ* is given in equation (5).

Where *Lxx(x, y, σ)* is the convolution of the second order derivative of Gaussian with image *I* at *(x,y)*. This also applies to *Lxy(x,y,σ)* and *Lyy(x,y,σ).*Scale spaces are usually implemented as an image pyramid. The images are repeatedly smoothed with a Gaussian and then sub-sampled in order to achieve a higher level of the pyramid.

Gaussians are optimal for scale-space analysis. In real applications, Gaussians have to be discretized and cropped. The SURF approximates the second order Gaussian derivate with box filters, which is calculated fast through integral images. The localization of interest point is determined by the determinant of Hessian matrix. So, interest points are finally localized in scale space and image space by using non-maximum suppression in their 3×3×3 neighbourhood. In the construction of descriptor of an interest point, a circular region around a detected interest point is first constructed. Then, a dominant orientation based on this circular region is calculated and assigned to this region, which enable the descriptor invariance to image rotations. The dominant orientation is calculated by the response of Haar wavelet. This process is also very fast by integral images. After the estimation of the dominant orientation, a square patch around an interest point is extracted to construct the SURF descriptor. The square patch is divided into a 4×4 sub-blocks. The gradients of each sub-block are used to construct the final descriptor vector.

IV. CLUSTERING

Clustering is the process of assigning a set of objects into groups so that the objects of similar type will be in one cluster. Clustering can be classified as hard clustering and soft clustering. Hard clustering and soft clustering differ in assigning the value to the partition matrix. Hard clustering assigns the value of either 0 or 1 whereas soft clustering allows the value to be in more than one cluster. The object will be assigned to a cluster that has the highest value. The general algorithms available for hard clustering are K-means [17] and K-medoid [18]. In this work hard clustering algorithms like K-means and K-medoid algorithms are used for clustering with Euclidean measure as distance metric learning.

A. *K means Algorithm*

K-meansis one of the simplest unsupervised algorithm that partition extracted features $(x_1 x_2, .., x_N)$ from images into *k* number of clusters. Given an image set *X*, initial random cluster centers are chosen.

B. *Steps for K means Algorithm*

The procedure follows in a simple way:

1) Compute the distances D_{ik}^2 between each data point $x_k$and cluster centers v_i.

$$D_{ik}^2 = (x_k - v_i)^T (x_k - v_i), \quad 1 \leq i \leq c, \quad 1 \leq k \leq N \quad (6)$$

2) Select the points for the cluster, with minimal distances, they belong to that cluster.

3) Recalculate the cluster centers $v_i^{(l)}$, by finding the mean of the data pointsx_i of corresponding clusters.

$$v_i^{(l)} = \frac{\sum_{j=1}^{N_i} x_i}{N_i} \quad (7)$$

until,

$$\prod_{k=1}^{n} max \left| v^{(l)} - v^{(l-1)} \right| \neq 0 \quad (8)$$

4) Repeat the process until *k* distinct clusters are obtained. Finally calculate the partition matrix.

C. *K- Medoid Algorithm*

The K-Medoid algorithm is a clustering algorithm related to the K-means algorithm and the medoid shift algorithm. Both the K-means and K-medoid algorithms

break the dataset up into groups and both attempt to minimize squared error, the distance between points labeled to be in a cluster and a point designated as the center of that cluster. In contrast to the K-means algorithm, K-medoid chooses data points as centers. K-medoid is also a partitioning technique of clustering that clusters the data set of n objects into k clusters with k known a priori. It is more robust to noise and outliers as compared to K-means because it minimizes a sum of general pairwise dissimilarities instead of a sum of squared Euclidean distances. The possible choice of the dissimilarity function is very rich but in this implementation the squared Euclidean distance is used.

D. Steps for K- Medoid Algorithm

A medoid of a finite dataset is a data point from this set, whose average dissimilarity to all the data points is minimal that is it is the most centrally located point in the set. Given the data set X, choose the number of clusters $1 < c < N$. Initialize with random cluster centers v_i chosen from the data set X.

1) Compute the distances D_{ik}^2 between each data point x_k and cluster centers v_i.

$$D_{ik}^2 = (x_k - v_i)^T (x_k - v_i), \quad 1 \le i \le c, \quad 1 \le k \le N \quad (9)$$

2) Associate each data point to the closest medoid.

3) Recalculate the cluster centers $v_i^{(l)*}$, by finding the mean of the data points x_i of corresponding clusters.

$$v_i^{(l)*} = \frac{\sum_{j=1}^{N_i} x_i}{N_i} \quad (10)$$

4) Choose the nearest data points to be the cluster center

$$D_{ik}^{i*} = (x_k - v_i^*)^T (x_k - v_i^*) \quad (11)$$

and

$$x_i^* = argmin_i \left(D_{ik}^{2*}\right);\ v_i^{(l)} = x_i^* \quad (12)$$

until

$$\prod_{k=1}^{n} max \left| v^{(l)} - v^{(l-1)} \right| \neq 0 \quad (13)$$

5) Repeat the process for l = 1, 2,.,..until k distinct clusters are obtained. Finally calculate the partition matrix.

K-medoidruns similar to K-means algorithm and this algorithm takes reduced computation time. This algorithmtests several methods for selecting initial medoid and calculates the distance matrix once.

V. CLASSIFIER

In pattern recognition, the k-nearest neighbor algorithm [19] (k-NN) is a method for classifying objects based on closest training examples in the feature space. The k-nearest neighbor algorithm is amongst the simplest of all machine learning algorithms. An object is classified by a majority vote of its neighbors where k is a positive integer, typically small. If k= 1, then the object is simply assigned to class of its nearest neighbor. The nearest-neighbor method is perhaps the simplest of all algorithms for predicting the class of a test example.

The training phase is simple, that is to store every training example, with its label. To make a prediction for a test example, first compute its distance to every training example. Then, keep the k closest training examples, where k ≥ 1 is a fixed integer. This basic method is called the k-NN algorithm. The most common distance function is Euclidean distance neighbors (k is a positive integer, typically small). If k= 1, then

$$d(x,y) = \|x - y\| = \sqrt{(x-y).(x-y)} = \sum_{j=1}^{m} (x_i - y_i)^2)^{1/2} \quad (14)$$

K-Nearest Neighbor algorithm (KNN) is a part ofsupervised learning that has been used in many applications inthe field of data mining, statistical pattern recognition andmany others. KNN is a method for classifying objects based on closest training examples in the feature vector. An object is classified by a majority vote of its neighbors. K is always a positive integer. The neighbors are taken from a set of objects for which the correct classification is known. It is usual to use the Euclidean distance, though other distance measures such as the Manhattan distance can be used.

VI. RESULTS AND DISCUSSION

The effect of different possible parameters and performance evaluation of Bag of visual words approach is done in terms of Precision, F1- measure and Accuracy rate for four different topics from dataset1 namely airplanes, cars, motorbikes and faces. Performance evaluation is also done for eight different topics namely burger, spaghetti, egg, spoon, bottle, can, coffee pot and mug of real world datasets that has been used in restaurant applications. Dataset1 is taken from Caltech database and since dataset2 is taken for real time application for visual recognition of objects used in restaurant,it is created from Google images. When compared to the images in dataset1 the size of images in dataset2 is comparatively small and can be categorized as tiny images when compared to dataset1.

The performance measures used in this evaluation are

1) Precision

$$P = \frac{1}{|c|}\sum_{i=1}^{|c|}\frac{TP_i}{TP_i+FP_i} \quad (15)$$

2) F1- measure

$$F = \frac{2 * P * R}{P + R} \quad (16)$$

where

$$R = \frac{1}{|c|}\sum_{i=1}^{|c|}\frac{TP_i}{TP_i+FN_i} \quad (17)$$

3) Accuracy rate

$$Accuracy = \frac{\sum_{i=1}^{c} TP_i+\sum_{i=1}^{c} TN_i}{\sum_{i=1}^{c}(TP_i+FN_i+FP_i+TN_i)} \quad (18)$$

In these equations TP indicates true positive, FP false positive, FN false negative and TN true negative of the classification result. Precision and recall are the most common measures for evaluating an information retrieval system. F1 score is a measure of test's accuracy. It considers both the precision P and recall R of the test to compute the score.The sample images of two different datasets are shown in Figure 2.

A performance evaluation of Bag of Words (BoW) is done using dataset1 and dataset2.The test data set includes four different topics in dataset1and eight topics in dataset2 each containing 50 images. 200 images per concept were used during the training phase to build the codebooks. The classifier is trained for another 200 images from each topic. The sizes of visual vocabularies are varied from 25 to 500 and evaluation performed. The distance measure used is Euclidean distance.

The parameters that affect the performance ofBoW are extraction of features and its description methods, dictionary generation methods, dictionary size, and distance function. A performance evaluation of four different combinations of parameters has been doneby varying the feature descriptor and dictionary generation method. The four combinations are (1) SIFT descriptor with K-means clustering (SIFTK-means) (2) SIFT descriptor with K-medoid clustering (SIFT K-medoid) (3) SURF descriptor with K-means clustering (SURF K-means) and (4) SURF descriptor with K-medoid clustering (SURF K-medoid). In the first two combinations Harris corner detector is used for feature extraction and in the next combinations Hessian detector is used. The distance function used in all implementation is Euclidean distance. KNN classifier is used for classifying the images. Evaluation is done by varying codebook size.

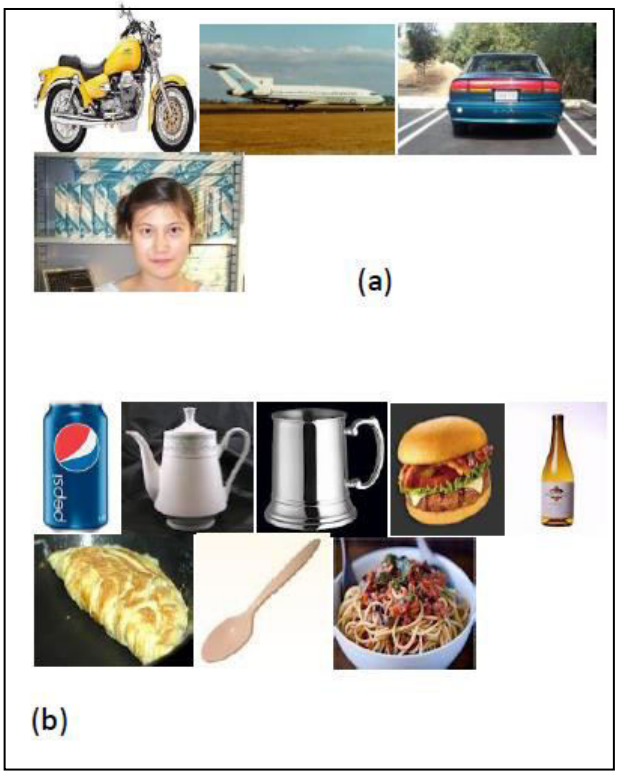

Figure.2 (a) sample images from dataset1 (b) sample images from dataset2

Among all, SURF K-means performs better for a codebook size of 100 for dataset1 and 500 for dataset2.In terms of run time K-medoid serves advantageous with reduced computation time. The results which give the effect of different possible parameters by varying codebook size for dataset1are shown in Table 1, 2 and Figure 3 and for dataset2 in Table 3, 4 and Figure 4. Sincedataset2 can be categorized as tiny image set when compared to dataset1 the performance measures of these image set is slightly less when compared to dataset1 as the number of features extracted depends on the size of the images. The performance measures can be further increased for Dataset2 by increasing the number of images from which features are extracted and trained.

TABLE I. Precision vs. Codebook Size for Dataset1

Codebook Size	*SIFT K-means*	*SIFT K-medoid*	*SURF K-means*	*SURF K-medoid*
25	0.75365	0.74215	**0.8571**	0.37364
50	0.8181	0.7715	**0.8828**	0.58628
75	0.85275	0.78945	**0.9123**	0.76951
100	0.8577	0.81935	**0.9271**	0.46384
200	0.9183	0.79725	**0.9056**	0.61672
300	0.9171	0.7675	**0.9132**	0.5873

TABLE II. F1 Measure vs. Codebook Size for Dataset1

Codebook Size	*SIFT K-means*	*SIFT K-medoid*	*SURF K-means*	*SURF K-medoid*
25	0.74676	0.7257	**0.8484**	0.37181
50	0.8064	0.7606	**0.8764**	0.58312
75	0.8438	0.7796	**0.9111**	0.75963
100	0.8513	0.80699	**0.926**	0.44896
200	0.9166	0.775	**0.9003**	0.6108
300	0.9135	0.769	**0.9066**	0.609

TABLE III. Precision vs. Codebook Size for Dataset2

Codebook Size	*SIFT K-means*	*SIFT K-medoid*	*SURF K-means*	*SURF K-medoid*
25	0.6872	0.68146	**0.66866**	0.48835
50	0.66456	0.6148	**0.71706**	0.5987
75	0.69277	0.64067	**0.73018**	0.56731
100	0.69863	0.68483	**0.74239**	0.52716
200	0.7048	0.68744	**0.71092**	0.575
300	0.6899	0.63899	**0.73874**	0.55026
400	0.67612	0.68638	**0.7577**	0.64355
500	0.6412	0.64744	**0.76873**	0.6479

TABLE IV. F1 Measure vs. Codebook Size for Dataset2

Codebook Size	*SIFT k-means*	*SIFT K-medoid*	*SURF K-means*	*SURF K-medoid*
25	0.67849	0.67568	**0.66176**	0.40945
50	0.65848	0.60463	**0.70327**	0.59305
75	0.68988	0.63529	**0.72123**	0.56236
100	0.68271	0.67219	**0.73359**	0.45621
200	0.69347	0.66687	**0.70287**	0.58109
300	0.68618	0.62935	**0.73308**	0.54252
400	0.67052	0.67552	**0.74875**	0.62235
500	0.633	0.62816	**0.75796**	0.6334

The maximum performance measures of four different combinations for dataset1 (Vehicular datasets) and dataset2 (Restaurant datasets) are shown in Table 5.

V. CONCLUSION

In this paper, the performance of Bag of visual words approach is investigated in terms of its degree of recognition using performance measures like accuracy rate, Precision and F1 measure. Dataset1 includes four different topics namely airplanes, cars, motorbikes and faces and dataset2 includes eight different topics namely burger, spaghetti, egg, spoon, bottle, can, coffee pot and mug of real world datasets that are commonly used in restaurant applications. The system presented here is based on visual vocabulary. The parameters that affect performance of Bag of Words (BoW) are, extracted features, description methods, dictionary generation methods, dictionary size, and distance function. A performance evaluation of four different combinations has been done by varying the feature descriptor and dictionary generation method. The four combinations are (1) SIFT descriptor with K-means clustering (SIFT K-means) (2) SIFT descriptor with K-medoid clustering (SIFT K-medoid) (3) SURF descriptor with K-means clustering (SURF K-means) and (4) SURF descriptor with K-medoid clustering (SURF K-medoid). Among all these combinations SURF K-means performs better for both the datasets.

TABLE V. Maximum performance measures for different methods for a given codebook size

Datasets	Method	Codebook Size	Max Accuracy Rate	Max. Precision	Max. F1 Measure
Dataset 1	*SIFT K-means*	200	0.9587	0.9183	0.9166
	SIFT K-medoid	100	0.8975	0.81935	0.80699
	SURF K-means	**100**	**0.9625**	**0.9271**	**0.926**
	SURF K-medoid	200	0.8025	0.61672	0.6108
Dataset 2	*SIFT K-means*	200	0.92063	0.7048	0.69347
	SIFT K-medoid	100	0.915	0.68483	0.67219
	SURF K-means	**500**	**0.93688**	**0.76873**	**0.75796**
	SURF K-medoid	400	0.90063	0.64355	0.62335

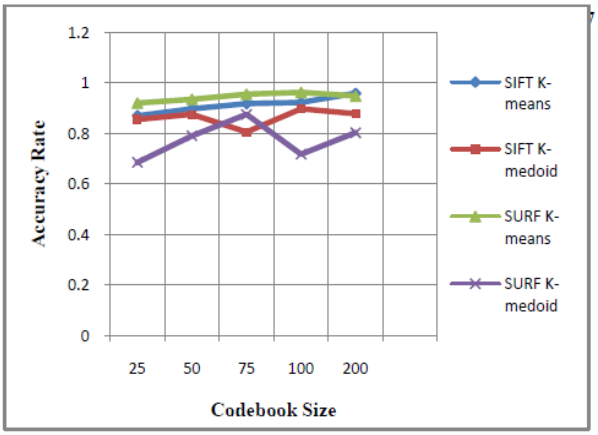

Figure.3 Accuracy Rate Vs Codebook Size for Dataset 1

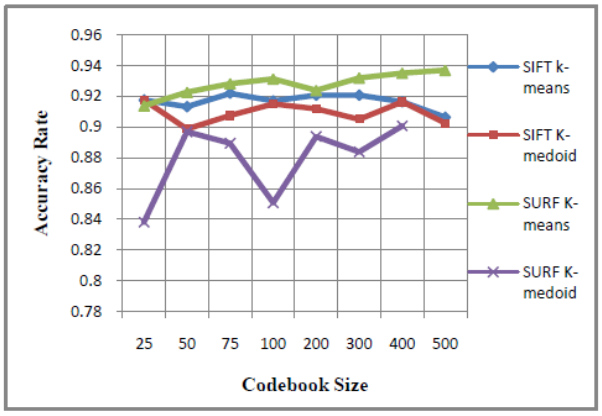

Figure.3 Accuracy Rate Vs Codebook Size for Dataset 2

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Designing of Test Facility
For High Rating Transformers

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Abstract - Testing of any electrical equipment after manufacture before installation is an essential feature. Especially testing of high rating transformers is a very difficult task as it requires a large value of voltage and current rating. To reduce the requirement of such a large value of voltage and current an attempt has been made in developing a test bench to suit for all varieties high rating transformers. The test bench consists of a motor generator set to develop the desired test voltage, a variable frequency drive(VFD) to increase or decrease the operating frequency, Test unit transformer (TUT) and intermediate transformer(IT), circuit breakers(CB) and capacitor bank to improve the power factor etc.,. This paper highlights the test bench preparation for testing of high rating transformers. The maximum rating of this test bench is 100MVA, but it can be used to test the transformers of 10MVA to 100MVA rating.

Keywords: *VFD, TUT, IT, CB*

I. INTRODUCTION

The power transformers are mainly used in the power generating stations where the transformer convert the power received at low voltage to power to be transmitted at high voltage as high voltage transmission is highly economical as for as losses, efficiency, voltage regulation are concerned. At the end of the transmission we incorporate distribution transformers to meet the local consumer's voltage levels. The basic requirement is testing of these transformers before they are installed. Testing is an important activity in the manufacturing of any equipment. Certain preliminary tests carried out at different stages of manufacture provide effective tool which assures quality and conformation to design calculations. The final tests on fully assembled transformer guarantee the stability of the equipment for satisfactory performance in service.

In the recent development of power systems the increase in the power capacity is the major achievement to the power industry. The power transmission in AC is --- kV and in DC it has reached 1200 kV. The power transformers are required at both the ends of the long transmission lines. That is one at the generating station and the other at the distribution end.

It is difficult to perform test on high rating power transformer, because of its higher ratings such as kVA, voltage and current. To overcome this difficulty, Experimental set up can be design to perform certain test i.e. loss measurement test, no load loss measurement test and temperature rise test.

Figure 1: Power Transformer

II. HARDWARE IMPLEMENTATION

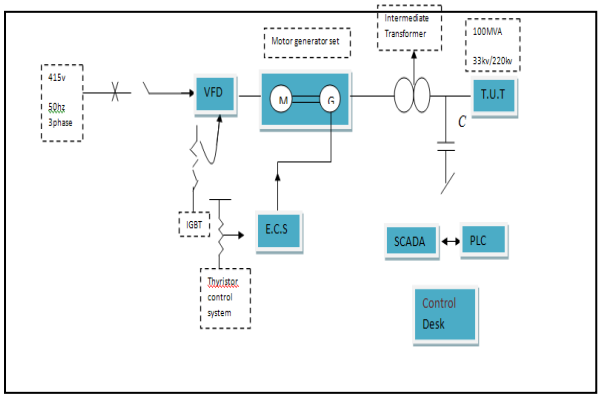

Fig 2: Test set up

The block diagram for test set up is shown in fig.2. It consists of TUT of rating 100MVA, 33/220kV to meet this requirement of primary TUT ratings an IT of rating 2.5 MVA, 1/33kV is used along with a capacitor bank to improve the power factor and reduce the kVA demand on generator. The transformer is supplied by AC MG set at constant frequency of 50Hz which is maintain throughout the test unit transformer with the help of VFD. The generator field is excited by Exciter control system to get the desired value of excitation

III. DESCRIPTION OF TEST UNIT BLOCKS

A. CIRCUIT BREAKERS (CB):

A circuit breaker is an automatically operated electrical switch designed to protect an electrical circuit from damage caused by overload or short circuit. Its basic function is to detect a fault condition and, by interrupting continuity, to immediately discontinue electrical flow. Unlike a fuse, which operates once and then has to be replaced, a circuit breaker can be reset (either manually or automatically) to resume normal operation.

Types of circuit breaker and their ratings are as follows:

a) Air Circuit Breaker (ACB); air at atmospheric pressure. From 690 to 1kV low voltage.

b) Vacuum Circuit Breaker (VCB) : From 3.3kV to 33kV medium voltage.

c) SF_6 Circuit Breakers: From 3.3kV to 800kV medium voltage.

These are the circuit breakers used in proposed work.

B. VARIABLE FREQUENCY DRIVES (VFD):

Variable frequency drive is a system for controlling the rotational speed of an AC electric motor by controlling the frequency of electric power applied to the motor these are called as Adjustable speed drives or Adjustable frequency drives.

Losses in the transformer are directly proportional to the number of cycle per second. By using VFD it is possible to set fine value of frequency i.e. 50Hz M-G set, hence test unit transformer will work at exactly 50Hz frequency.

Benefits of VFD

Variable frequency drives provide the following advantages:

- Energy savings
- Low motor starting current
- Reduction of thermal and mechanical stresses on motors and belts during starts
- Simple installation
- High power factor
- lower KVA

C. MOTOR-GENERATOR SET:

Motor and Generator set will provide required voltage to the intermediate transformer at frequency 50Hz throughout the test. Frequency can be adjusted to exact 50Hz by variable frequency drive. Hence motor runs at rated speed, generator is mechanically coupled to motor there by generator also runs at same speed as that of motor. Generator field is excited by exciter control system.

CONVERSIONS:

Motor-generators may be used for various conversions including:

- Alternating current (AC) to direct current (DC)
- DC to AC
- DC at one voltage to DC at another voltage
- AC at one frequency to AC at nother harmonically-related frequency
- AC at a fixed voltage to AC of a variable voltage

D. EXCITER CONTROL SYSTEM:

Excitation systems have a powerful impact on generator dynamic performance and availability, it ensures quality of generator voltage and reactive power, i.e. quality of delivered energy to consumers. Following types are common:

- Brushless excitation systems, with rotating exciter machines and Automatic Voltage Regulator (AVR), or
- Static excitation systems (SES), feeding rotor directly from thyristor bridges via brushes.

Main functions of excitation system are to provide variable DC current with short time overload capability, controlling terminal voltage with suitable accuracy, ensure stable operation with other machines, to keep machine within permissible operating range.

E. SCADA and PLC:

Supervisory Control and Data Acquisition (SCADA) Systems are used to monitor and control a test set up.

SCADA systems consist of:

- One or more field data interface devices,
- A communications system used to transfer data
- A central host computer server or servers

A programmable logic controller (PLC) or programmable controller is a digital computer used for automation of electromechanicalprocesses, such as control of machinery on factory assembly lines, amusement rides, or light fixtures. PLCs are used in many industries and machines. Unlike general-purpose computers, the PLC is designed for multiple inputs and output arrangements, extended temperature ranges, immunity to electrical noise, and resistance to vibration and impact. Programs to control machine operation are typically stored in battery-backed-up or non-volatile memory. A PLC is an example of a hard real time system since output results must be produced in response to input conditions within a limited time, otherwise unintended operation will result.

IV. SYSTEM DESIGN:

Procedure for calculation

Impedance voltage Vz %

Primary voltage of test unit transformer Vp

Secondary voltage of test unit transformer Vs

KVA rating of test unit transformer $(KVA)_{TUT}$

Test unit transformer efficiency n

Supply frequency f=50 Hz

Generator efficiency n_g

Motor efficiency n_m

VFD efficiency n_v

Line power factor PF_L

P= number of poles in motor and generator

Impedance voltage v_z = Vp * %Vz

Primary current $i_p = \frac{(KVA)TUT}{\sqrt{3}*Vp}$

Required KVA uncompensated = $\sqrt{3} * Vz * ip$

Loss "w" = $( )TUT * \frac{1-n}{100}$

Power factor = $\frac{w}{(KVA)uc} = \cos\emptyset$

$\emptyset = \cos^{-1}[\frac{w}{(KVA)uc}]$

$\sin\emptyset = \sin[\frac{w}{(KVA)uc}]$

Active current = $i_a = i_p * \cos\emptyset$

Reactive current = $i_r = i_p * \sin\emptyset$

For 85% of line current = $i_r * 0.85 = i_c$

$$I_{rms} = \sqrt{ia^2 + (ir - ic)^2}$$

Current supplied by intermediate transformer is Irms

KVA supplied by intermediate transformer and generator is given by

$(KVA)_{IT} = \sqrt{3} * Vz * Irms$

Power factor = $\frac{ia}{Irms} = \cos\emptyset 1$

Reactive power is given by KVAR

KVAR = $\sqrt{3} * Vz * i_c$

Capacitor design:

Capacitor current $i_{ca} = \frac{KVAR}{\sqrt{3} * Vz}$

Capacitor reactance = Xc = $\frac{Vz}{ia}$

Capacitor "C" = $\frac{1}{2\pi f Xc}$

Generator design:

Required KW of generator = $(KVA)_{IT} * \cos\emptyset 1$ = KW

Considering factor of safety in KW = (KW) * 2 = (KW)ge

Output of generator in KW = (KW)ge

Input to the generator = $\frac{(KW)ge}{ng}$

Motor design:

Output of motor = input to the generator.

Input to the motor = $\frac{(KW)m}{nm}$

VFD design:

VFD output = motor input

VFD input = $\frac{(KW)v}{nv} = (KW)_{VFD}$

Line KVA = $\frac{VFD\ input}{line\ power\ factor} = (KVA)_L$

Line current = $\frac{(KVA)l}{\sqrt{3} * Vl}$

Motor:

P = $\frac{120f}{N}$

$$Nm = \frac{120f}{P}$$

Generator : $$Fg = \frac{Pg*Nm}{120}$$

V. TESTS

A. No load loss measurement test.

The purpose is to carry out the measurement of no-load loss of the transformer at specified no-load conditions and establish that the measured no-load loss confirms to the designed and guaranteed figures within the specified tolerances. The average magnetizing current of the transformer, which may form of part of guaranteed parameters in special cases. The measurement of no load loss is important not only for purpose of assessing the efficiency of the transformer, but also as a check that the high voltage test have not caused any damage to winding insulation.

The secondary of the transformer is left open-circuited. A wattmeter is connected to the primary. An ammeter is connected in series with the primary winding. A voltmeter is optional since the applied voltage is same as the voltmeter reading. Rated voltage is applied at primary.

If the applied voltage is normal voltage then normal flux will be set up. As the Iron loss is a function of applied voltage, normal iron loss will occur. Hence the iron loss is maximum at rated voltage. This maximum iron loss is measured using the wattmeter. Since the impedance of the series winding of the transformer is very small compared to that of the excitation branch, all of the input voltage is dropped across the excitation branch. Thus the wattmeter measures only the iron loss. It should be noted that the iron losses consist of the hysteresis loss and the eddy current loss. This test only measures the combined loss. Although the hysteresis loss is less than the eddy current loss, it is not negligible. The two losses can be separated by driving the transformer from a variable frequency source since the hysteresis loss varies linearly with supply frequency and the eddy current loss varies with the square.

Since the secondary of the transformer is open, the primary draws only no load current which will have some copper loss. This no load current is very small and because the copper loss in the primary is proportional to the square of this current, it is negligible. There is no copper loss in the secondary because there is no secondary current.

B. Loss measurement test.

The purpose is to carry out the measurement of load loss and impedance of the transformer at specified load conditions and establish that the derived load loss and impedance figures conform to the designed and guaranteed figures within the specified tolerances. The goals achieved at the end of the test are, the impedance voltage corresponding to the applied currents at the temperature of measurement · The total load loss at the temperature of measurement.

This is mainly due to ohmic resistance of transformer winding. Copper loss also includes the stray loss occurring in the mechanical structure and winding conductor due to the stray fluxes. Copper loss is measured by short circuit test.

The test is conducted on the high voltage (HV) side of the transformer where the low voltage (LV) side or the secondary is short circuited. The supply voltage required to circulate rated current through the transformer is usually very small and is of the order of a few percent of the nominal voltage and this voltage is applied across primary. The core losses are very small because applied voltage is only a few percentage of the nominal voltage and hence can be neglected. Thus the wattmeter reading measures only the full load copper loss

C. Temperature rise test.

The test is conducted to confirm that under normal conditions, the temperature rise of the windings and the oil will not exceed the specified limit. The temperature rises are measured above the temperature of the cooling air, for all types of transformers except those water cooled.

Temperature-rise test is a type test. The oil and winding temperatures are tested whether they are in accordance with both standards and technical specifications or not.

VI. CONCLUSION

By designing test set up it possible to conduct loss measurement test, no load loss measurement test and temperature rise test on the high rating transformer. The maximum rating of this test bench is 100MVA, but it can be used to test the transformers of 10MVA to 100MVA rating.

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